LVDS Product

DTC35LM35 (Rev. 1.3)

REVISED MAY. 2007

+3.3V LVDS 30Bit Flat Panel Display (FPD) Transmitter - 135MHz

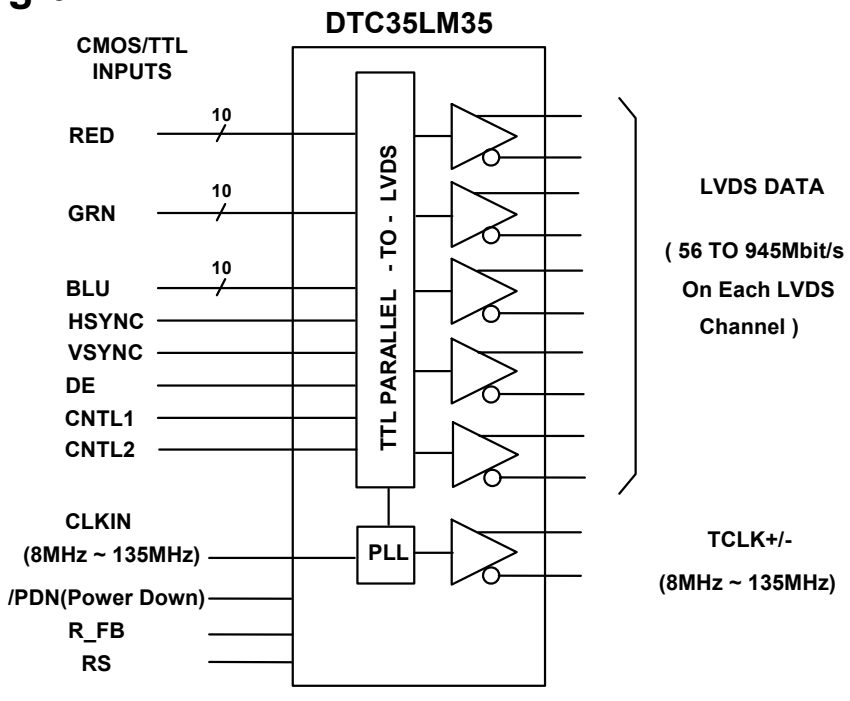
General Description

The DTC35LM35 transmitter converts 35 bits of CMOS/TTL data into five LVDS(Low Voltage Differential Signaling) data streams. A CLKIN signal is phase-locked and transmitted in parallel with the data streams over a sixth LVDS link. 30 bits of graphic data and 3 bits(HSYNC, VSYNC,DE) of timing and 2 control data(CNTL1,CNTL2) are transmitted at a rate of 945 Mbps per LVDS data channel at a transmit clock frequency of 135MHz. Using a 135 MHz clock, the data throughput is 590.6 Mbytes/sec. The R_FB pin selects either rising or falling edge trigger of CLKIN. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

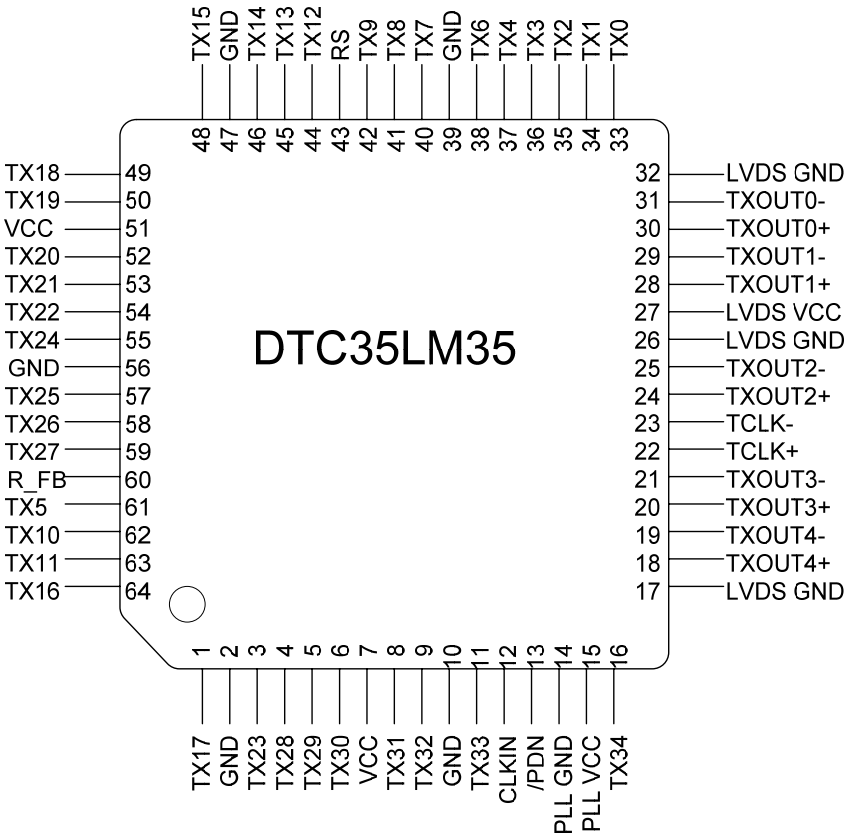
Features

- Wide frequency range : 8 to 135 MHz shift clock support
- Single 3.3V supply
- Power-Down Mode
- Supports NTSC,VGA, SVGA, XGA ,SXGA and SXGA+
- Supports Spread Spectrum Clock Generator
- On Chip Input Jitter Filtering
- Up to 590.6 Megabytes/sec bandwidth
- Up to 4.72 Gbps throughput
- 345mV swing LVDS devices for low EMI
- PLL requires no external components
- 64Pin TQFP package
- Pin compatible with Thine THC63LVD103
- Backward compatible with DTC33LM85AL(18Bits) / DTC34LM85AL(24Bits)

Block Diagram

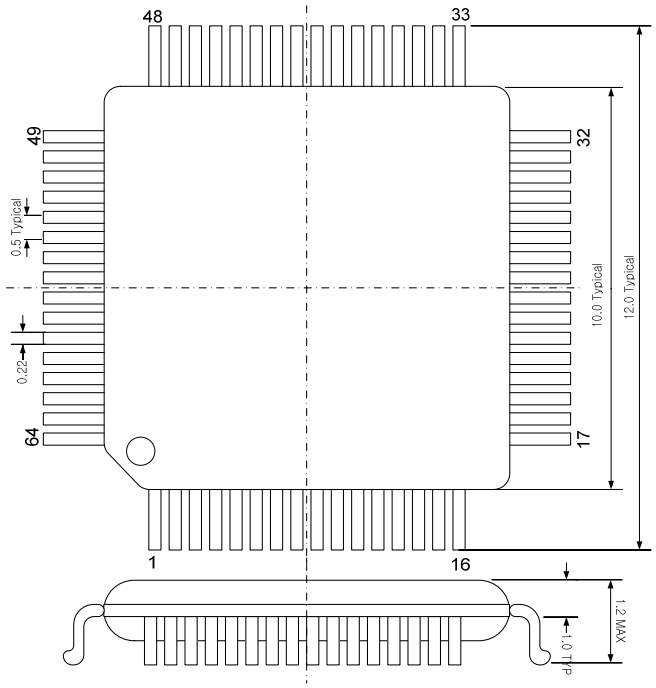


PIN OUT



PACKAGE

64 Pin TQFP Package, JEDEC [Unit : millimeters]



Electrical Characteristics

Vcc=3.0 ~ 3.6V, Ta=-10 ~ +70°C

CMOS/TTL DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	RS=VCC or GND	2.0		Vcc	V
V_{IL}	Low Level Input Voltage	RS=VCC or GND	GND		0.8	V
V_{DDQ}	Small Swing Voltage		1.2		2.8	V
V_{REF}	Input Reference voltage	Small Swing(RS= V_{DDQ}/2)		V_{DDQ}/2		V
		CMOS(RS=VCC or GND)		VCC		V
V_{IH_S}	High Level Input Voltage(Small)	VREF= V_{DDQ}/2	V_{DDQ}/2 +0.1V			V
V_{IL_S}	Low Level Input Voltage(Small)	VREF= V_{DDQ}/2			V_{DDQ}/2 -0.1V	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ Vcc			±10	uA
I_{PD}	Pull Down Current	R/FB pin, VIH=Vcc			10	uA

LVDS TRANSMITTER DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage, Normal RS=VCC (Small RS=GND)	RL=100Ω	250 (100)	350 (200)	450 (300)	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between Complimentary Output States				35	mV
I_{OZ}	Output TRI-STATE Current	/PDN=0V, Vout=0 to Vcc			±10	uA

TRANSMITTER SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{TG}	Transmitter Supply Current (Grayscale)	RL=100Ω, CL = 5pF, f = 85MHz, RS=VCC (RS=GND)	55 (42)	68 (52)	mA
		RL=100Ω, CL = 5pF, f = 135MHz, RS=VCC (RS=GND)	68 (54)	79 (65)	mA
ICC_{TW}	Transmitter Supply Current (Worst Case)	RL=100Ω, CL = 5pF, f = 85MHz, RS=VCC (RS=GND)	67 (52)	77 (63)	mA
		RL=100Ω, CL = 5pF, f = 135MHz, RS=VCC (RS=GND)	85 (71)	96 (82)	mA
ICC_{TP}	Transmitter Supply Current (Power Down)	/PDN=0V	10		uA

* All typical values are Vcc = 3.3V, Ta = 25°C

Absolute Maximum Ratings (Note1)

Supply Voltage (Vcc)	-0.3 to +4.0V
CMOS/TTL Input Voltage	-0.3V to (Vcc + 0.3V)
CMOS/TTL Output Voltage	-0.3V to (Vcc + 0.3V)
LVDS Driver Output Voltage	-0.3V to (Vcc + 0.3V)
Output Short Circuit Duration	Continuous
Junction Temperature	+150 °C
Storage Temperature Range	-65 °C to 150 °C
Lead Temperature (Soldering, 4 sec.)	+260 °C
Maximum Power Dissipation @25°C	1.4W

(Note 1)

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation

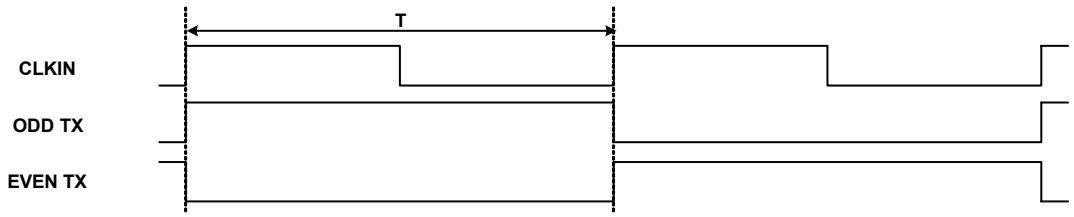
Transmitter Switching Characteristics

Vcc=3.0 ~ 3.6V, Ta=-10 ~ +70°C, T=1/f

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLKIN Transition Time			5.0	nS
t_{TCP}	CLKIN Period	7.4	T	125.0	nS
t_{TCH}	CLKIN High Time	0.35T	0.5T	0.65T	nS
t_{TCL}	CLKIN Low Time	0.35T	0.5T	0.65T	nS
t_{TCD}	CLKIN to TCLK+/- Delay		2T/7 + 2.3		nS
t_{TS}	TTL Data Setup to CLKIN	2.5			nS
t_{TH}	TTL Data Hold from CLKIN	2.5			nS
t_{LVT}	LVDS Transition Time		0.6	1.5	nS
t_{TDP1}	Transmitter Output Data Position 0	-0.2	0	0. 2	nS
t_{TDP0}	Transmitter Output Data Position 1	T/7-0. 2	T/7	T/7+0. 2	nS
t_{TDP6}	Transmitter Output Data Position 2	2T/7-0. 2	2T/7	2T/7+0. 2	nS
t_{TDP5}	Transmitter Output Data Position 3	3T/7-0. 2	3T/7	3T/7+0. 2	nS
t_{TDP4}	Transmitter Output Data Position 4	4T/7-0. 2	4T/7	4T/7+0. 2	nS
t_{TDP3}	Transmitter Output Data Position 5	5T/7-0. 2	5T/7	5T/7+0. 2	nS
t_{TDP2}	Transmitter Output Data Position 6	6T/7-0. 2	6T/7	6T/7+0. 2	nS
t_{TPLLS}	Transmitter Phase Lock Loop Set	-	-	10	mS

AC Timing Diagrams

FIGURE 1. Test Pattern "Worst Case Pattern"



AC Timing Diagrams(Continued)

FIGURE 2. Test Pattern "Grayscale Test Pattern"

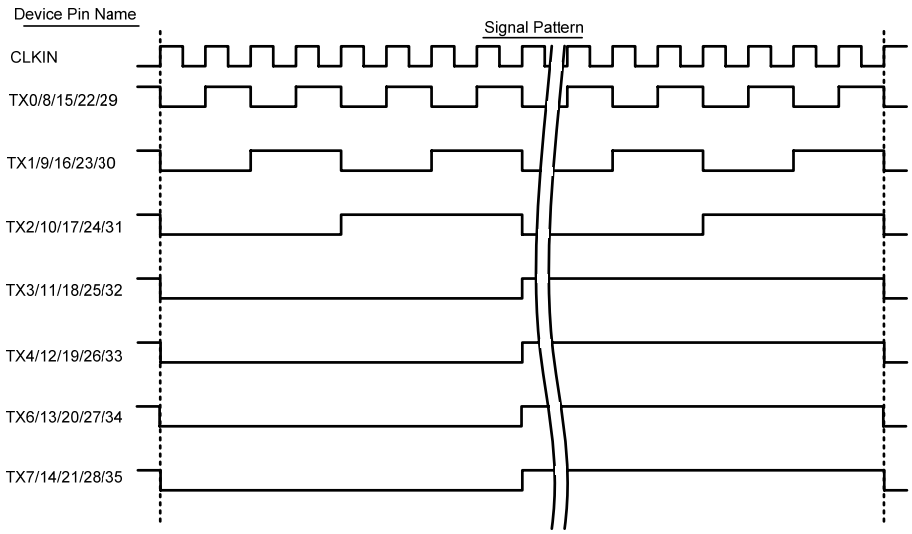


FIGURE 3. TTL Input

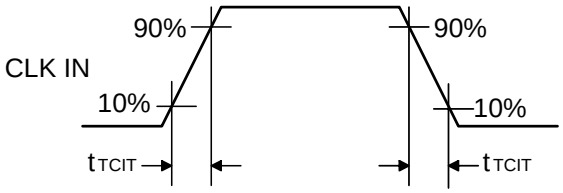
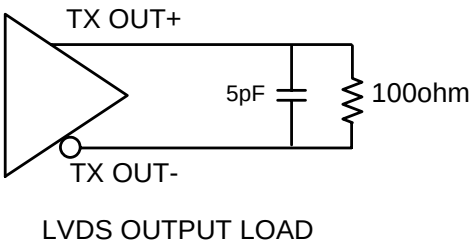
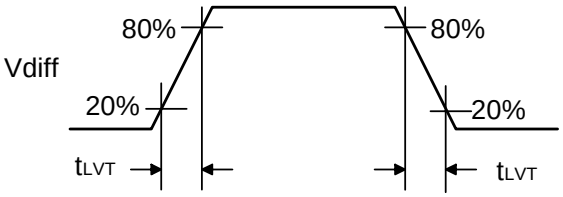


FIGURE 4. LVDS Output

Vdiff= (TXOUT+) – (TXOUT–)



LVDS OUTPUT LOAD



AC Timing Diagrams (Continued)

FIGURE 5. Phase Lock Loop Set Time

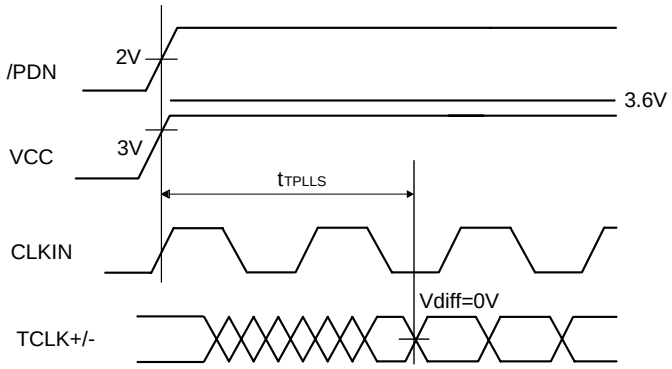
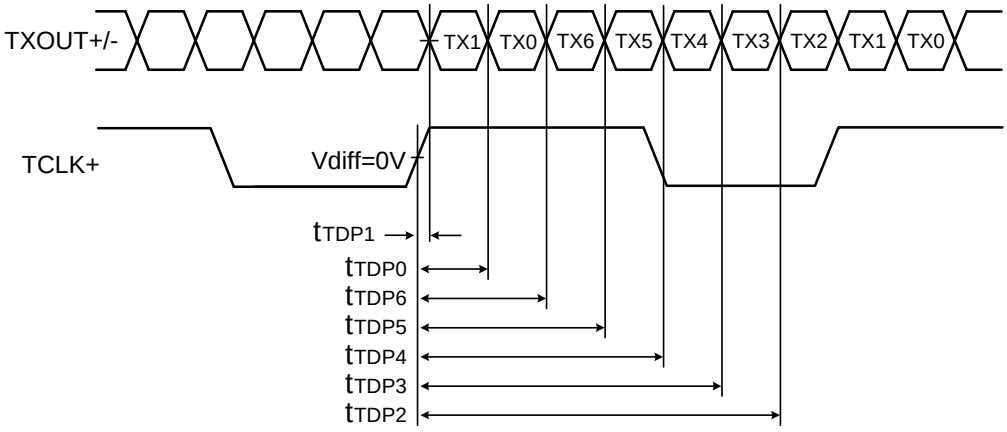


FIGURE 6. Transmitter Device Operation



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) – (TCLK-)**

FIGURE 7. Parallel TTL Data Inputs Mapped to LVDS Outputs

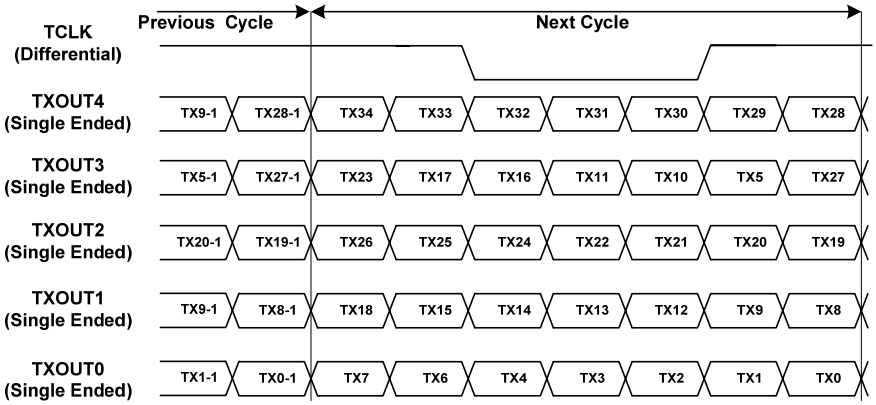
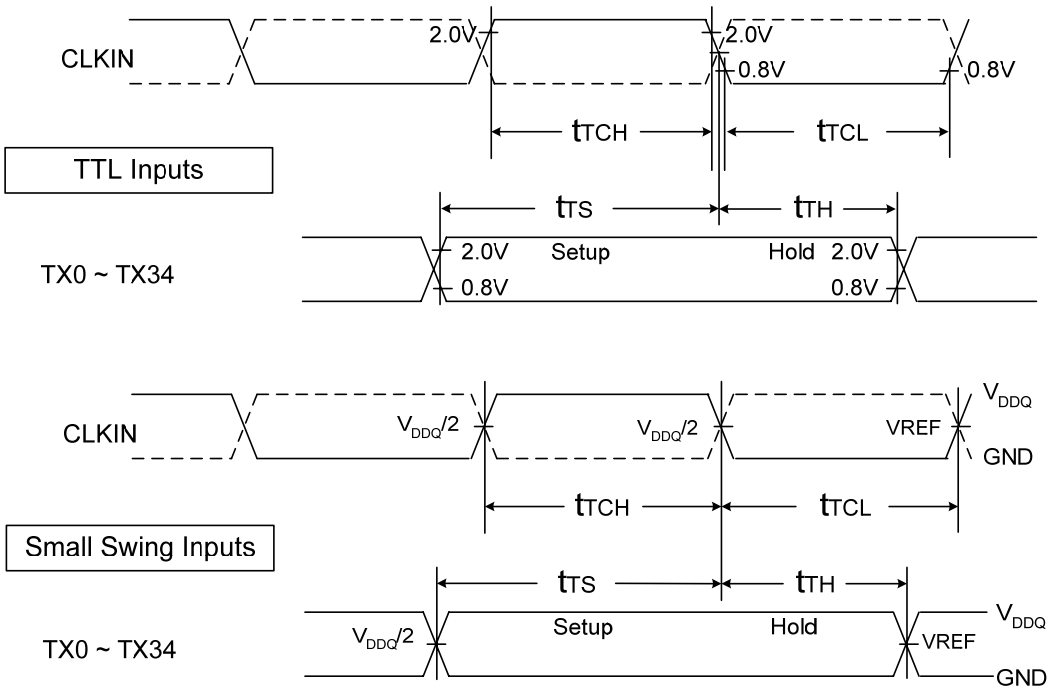


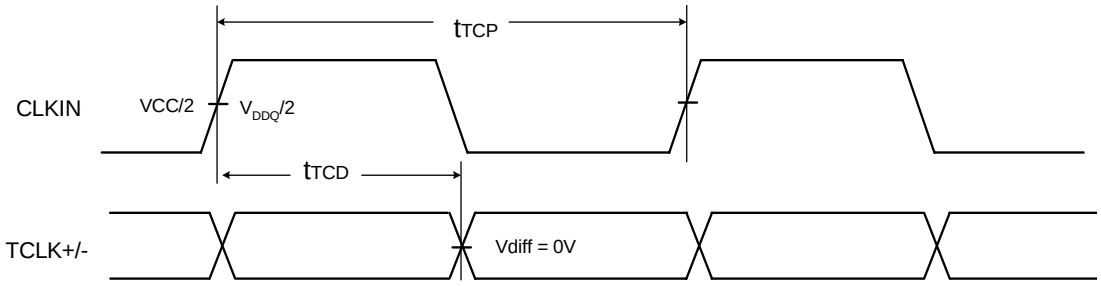
FIGURE 8. Setup/Hold and High/Low Times



Note : **1) CLKIN : for DTC35LM35(R_FB=GND), denoted as solid line**

for DTC35LM35(R_FB=VCC), denoted as dotted line

FIGURE 9. CLKIN to CLKOUT Delay



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) - (TCLK-)**

FIGURE 10. Package Pin Description

Pin Name	Pin #	Type	Description
TXOUT0-, TXOUT0+	31, 30	LVDS OUT	LVDS differential data outputs.
TXOUT1-, TXOUT1+	29, 28	LVDS OUT	
TXOUT2-, TXOUT2+	25, 24	LVDS OUT	
TXOUT3-, TXOUT3+	21, 20	LVDS OUT	
TXOUT4-, TXOUT4+	18, 19	LVDS OUT	
TCLK+, TCLK-	23, 22	LVDS OUT	LVDS differential clock outputs.
TX0 ~ TX6	33,34,35,36,37,61,38	IN	TTL level data inputs. This includes : 10 Red, 10 Green, 10 Blue, and 5 control lines (HSYNC, VSYNC, DE, CNTL1,CNTL2)
TX7 ~ TX13	40,41,42,62,63,44,45	IN	
TX14 ~ TX20	46,48,64,1,49,50,52	IN	
TX21 ~ TX27	53,54,3,55,57,58,59	IN	
TX28 ~ TX34	4,5,6,8,9,11,16	IN	
CLK IN	12	IN	TTL level clock input. This falling edge acts as data strobe
/PDN	13	IN	TTL level input. H : Normal operation L : Power down (all output are low)
R_FB	60	IN	Programmable strobe select. H:Rising edge, L :Falling edge
RS	43	IN	Small Swing mode (Input Reference)
VCC	51.7	Power	Power supply pins for TTL inputs.
GND	2,10,39,47,56	Ground	Ground pins for TTL inputs.
LVDS VCC	27	Power	Power supply pin for LVDS outputs.
LVDS GND	17,26,32	Ground	Ground pins for LVDS outputs.
PLL VCC	15	Power	Power supply pin for PLL.
PLL GND	14	Ground	Ground pin for PLL.

Table 1. Bit Mapping for 30-bit , 24-bit and 18-bit Color Display

VGA-TFT Data Signal				Transmitter Input Data Pin		
	30-bit	24-bit	18-bit	30-bit (35LM35)	24-bit Tx (34LM85A)	18-bit Tx (33LM85A)
LSB	R0	-	-	TX28	-	-
	R1	-	-	TX29	-	-
	R2	R2	-	TX27	TX27	-
	R3	R3	-	TX5	TX5	-
	R4	R4	R4	TX0	TX0	TX0
	R5	R5	R5	TX1	TX1	TX1
	R6	R6	R6	TX2	TX2	TX2
	R7	R7	R7	TX3	TX3	TX3
	R8	R8	R8	TX4	TX4	TX4
MSB	R9	R9	R9	TX6	TX6	TX6
LSB	G0	-	-	TX30	-	-
	G1	-	-	TX31	-	-
	G2	G2	-	TX10	TX10	-
	G3	G3	-	TX11	TX11	-
	G4	G4	G4	TX7	TX7	TX7
	G5	G5	G5	TX8	TX8	TX8
	G6	G6	G6	TX9	TX9	TX9
	G7	G7	G7	TX12	TX12	TX12
	G8	G8	G8	TX13	TX13	TX13
MSB	G9	G9	G9	TX14	TX14	TX14
LSB	B0	-	-	TX32	-	-
	B1	-	-	TX33	-	-
	B2	B2	-	TX16	TX16	-
	B3	B3	-	TX17	TX17	-
	B4	B4	B4	TX15	TX15	TX15
	B5	B5	B5	TX18	TX18	TX18
	B6	B6	B6	TX19	TX19	TX19
	B7	B7	B7	TX20	TX20	TX20
	B8	B8	B8	TX21	TX21	TX21
MSB	B9	B9	B9	TX22	TX22	TX22
	Hsync	Hsync	Hsync	TX24	TX24	TX24
	Vsync	Vsync	Vsync	TX25	TX25	TX25
	DE	DE	DE	TX26	TX26	TX26
	N/A	N/A	-	TX23	TX23	-
	N/A	-	-	TX34	-	-

IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.

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