LVDS Product

DTC33LM85AL *(Rev. 1.0)*

REVISED APR. 2009

+3.3V LVDS 18Bit Flat Panel Display (FPD) Transmitter - 85MHz

General Description

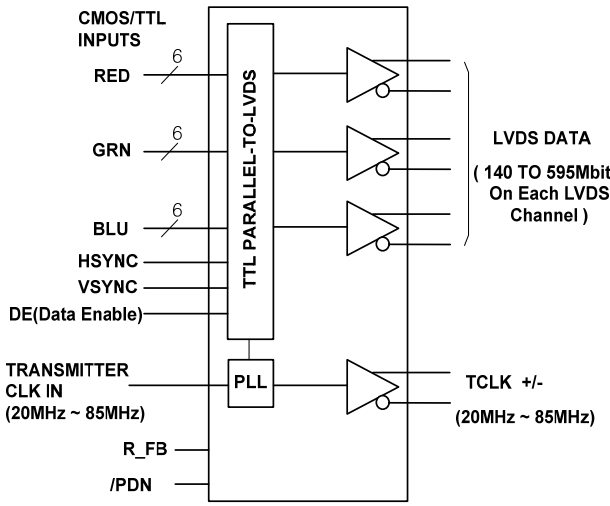
The DTC33LM85AL transmitter converts 21 bits of CMOS/TTL data into three LVDS(Low Voltage Differential Signaling) data streams. A CLKIN signal is phase-locked and transmitted in parallel with the data streams over a fourth LVDS link. 18 bits of graphic data and 3 bits of timing are transmitted at a rate of 595 Mbps per LVDS data channel at a transmit clock frequency of 85MHz. Using a 85 MHz clock, the data throughput is 223 Mbytes/sec. The R_FB pin selects either rising or falling edge trigger of CLKIN. A Rising/Falling edge strobe transmitter will interoperate with a Rising/Falling edge strobe receiver (DTC33LF/R86L) without any translation logic. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

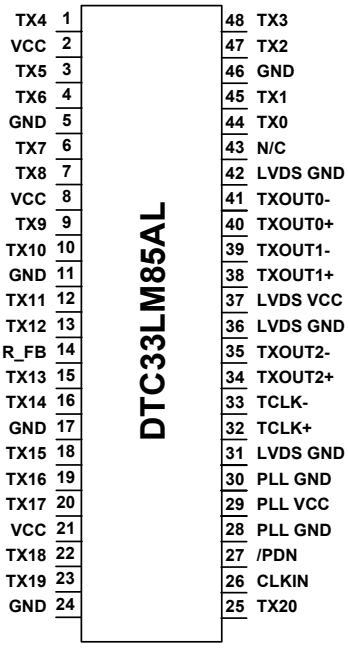
- Wide frequency range : 20 to 85 MHz shift clock support
- Narrow bus (8 lines) reduces cable size and cost
- Single 3.3V supply
- Power-Down Mode
- Supports VGA, SVGA, XGA and SXGA
- Supports Spread Spectrum Clock Generator
- On Chip Input Jitter Filtering
- Up to 223 Megabytes/sec bandwidth
- Up to 1.785 Gbps throughput
- 345mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 48-lead TSSOP package (PB Free)
- Compatible with TIA/EIA-644 LVDS standard
- Compatible with National DS90C365
  Thine THC63LVDM63A

Block Diagram

DTC33LM85AL



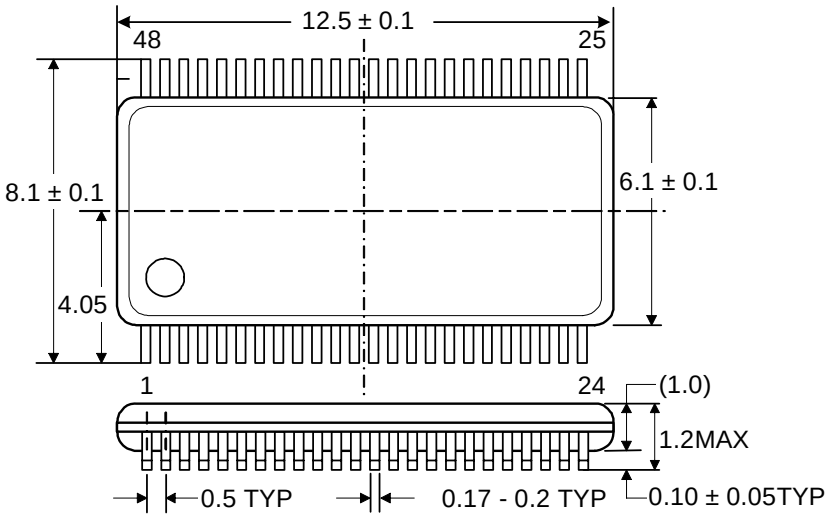
PIN OUT



PACKAGE

48 Lead Molded Thin Shrink Small Outline Package, JEDEC

Unit : millimeters



Electrical Characteristics

Vcc=3.0 ~ 3.6V, Ta=-10 ~ +70°C

CMOS/TTL DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		Vcc	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq Vcc$			+/- 10	uA
I_{PD}	Pull Down Current	R/FB pin, VIH=Vcc			10	mA

LVDS TRANSMITTER DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	RL=100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	Vout=0V,RL=100Ω		- 3.5	5	uA
I_{OZ}	Output TRI-STATE Current	/PDN=0V, Vout=0 to Vcc			±10	uA

TRANSMITTER SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{TG}	Transmitter Supply Current (16 Grayscale)	RL=100Ω, CL = 10pF, f = 85MHz 16 Grayscale Pattern	35		mA
ICC_{TW}	Transmitter Supply Current (Worst Case)	RL=100Ω, CL = 10pF, f = 85MHz Worst Case Pattern	37		mA
ICC_{TP}	Transmitter Supply Current (Power Down)	/PDN=0V	10		uA

* All typical values are Vcc = 3.3V, Ta = 25°C

Absolute Maximum Ratings (Note1)

Supply Voltage (Vcc) -0.3 to +4.0V
CMOS/TTL Input Voltage -0.3V to (Vcc + 0.3V)
CMOS/TTL Output Voltage -0.3V to (Vcc + 0.3V)
LVDS Driver Output Voltage -0.3V to (Vcc + 0.3V)
Output Short Circuit Duration Continuous
Junction Temperature +150 °C
Storage Temperature Range -65 °C to 150 °C
Lead Temperature (Soldering, 4 sec.) +260 °C
Maximum Power Dissipation @25°C 1.4W

(Note 1)

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation

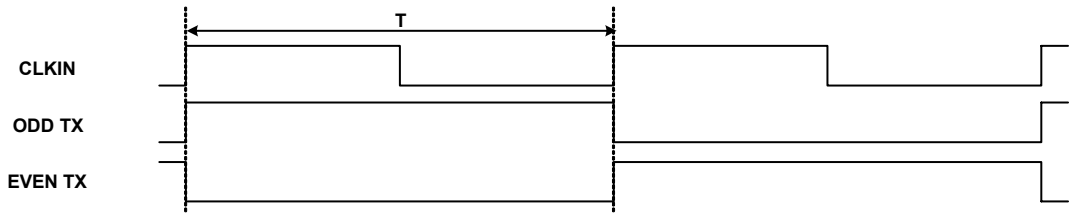
Transmitter Switching Characteristics

Vcc=3.0 ~ 3.6V, Ta=-10 ~ +70°C, T=1/f

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLKIN Transition Time			5.0	
t_{TCP}	CLKIN Period	11.76	T	50	nS
t_{TCH}	CLKIN High Time	0.35T	0.5T	0.65T	nS
t_{TCL}	CLKIN Low Time	0.35T	0.5T	0.65T	nS
t_{TCD}	CLKIN to TCLK+/- Delay		2T/7 + 2.3		nS
t_{TS}	TTL Data Setup to CLKIN	2.5			nS
t_{TH}	TTL Data Hold from CLKIN	2.5			nS
t_{LVT}	LVDS Transition Time		0.6	1.5	nS
t_{TDP1}	Transmitter Output Data Position 0 (85MHz)	-0.2	0	0. 2	nS
t_{TDP0}	Transmitter Output Data Position 1 (85MHz)	T/7-0. 2	T/7	T/7+0. 2	nS
t_{TDP6}	Transmitter Output Data Position 2 (85MHz)	2T/7-0. 2	2T/7	2T/7+0. 2	nS
t_{TDP5}	Transmitter Output Data Position 3 (85MHz)	3T/7-0. 2	3T/7	3T/7+0. 2	nS
t_{TDP4}	Transmitter Output Data Position 4 (85MHz)	4T/7-0. 2	4T/7	4T/7+0. 2	nS
t_{TDP3}	Transmitter Output Data Position 5 (85MHz)	5T/7-0. 2	5T/7	5T/7+0. 2	nS
t_{TDP2}	Transmitter Output Data Position 6 (85MHz)	6T/7-0. 2	6T/7	6T/7+0. 2	nS
t_{TPLLS}	Transmitter Phase Lock Loop Set	-	-	10	mS

AC Timing Diagrams

FIGURE 1. Test Pattern "Worst Case Pattern"



AC Timing Diagrams(Continued)

FIGURE 2. Test Pattern "16 Grayscale Test Pattern"

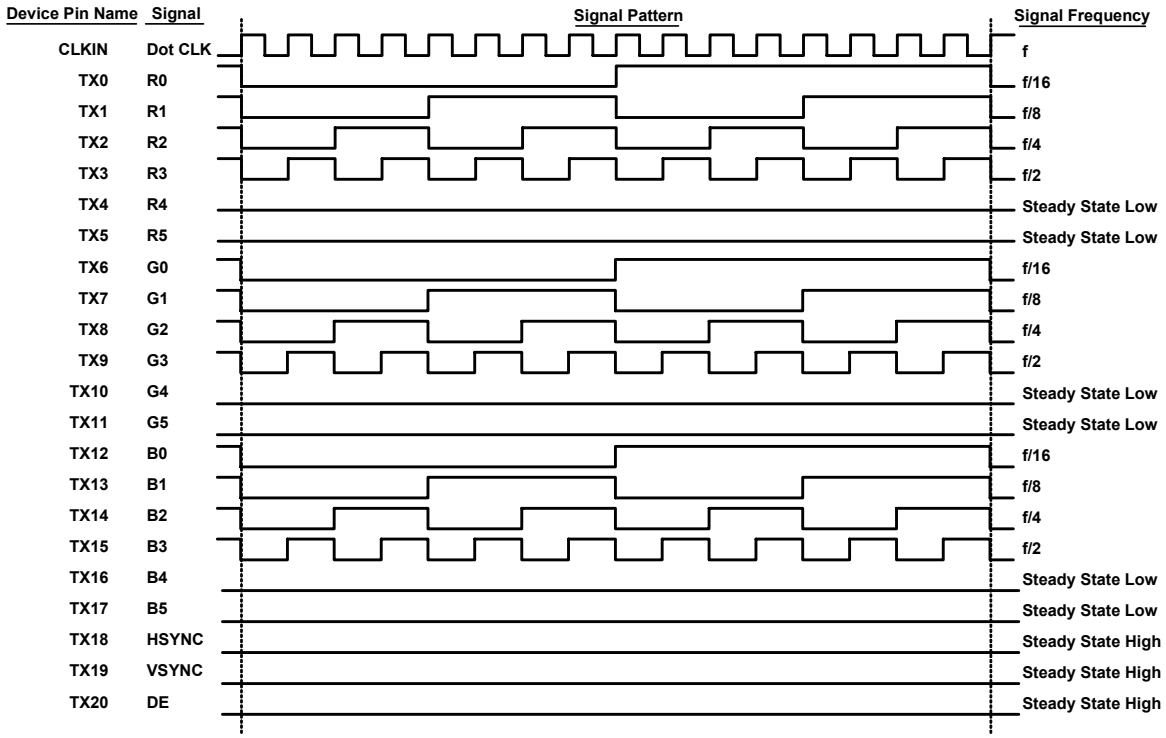


FIGURE 3. TTL Input

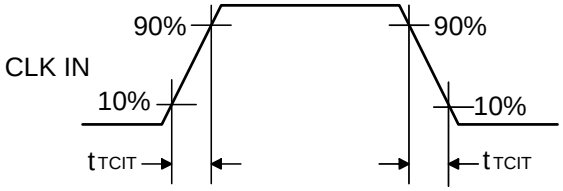
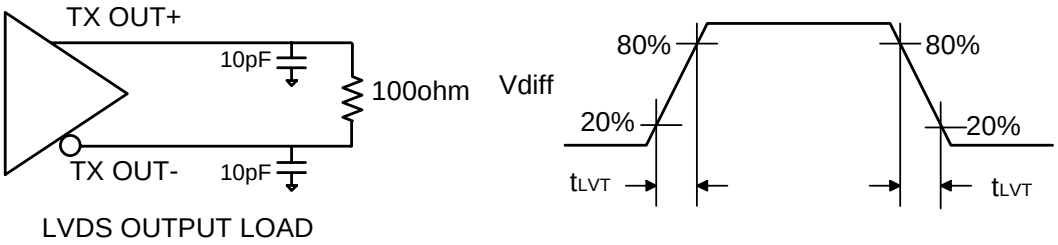


FIGURE 4. LVDS Output

Vdiff= (TXOUT+) – (TXOUT–)



AC Timing Diagrams (Continued)

FIGURE 5. Phase Lock Loop Set Time

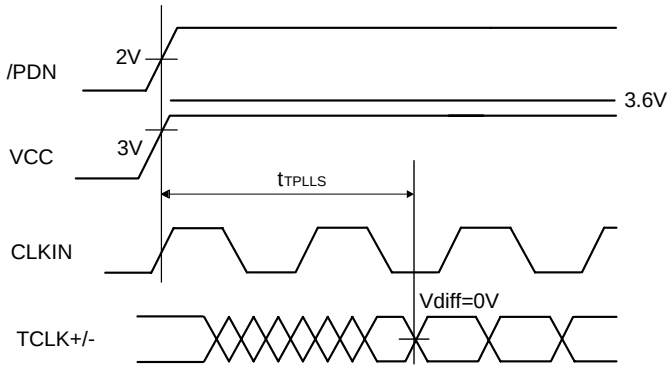
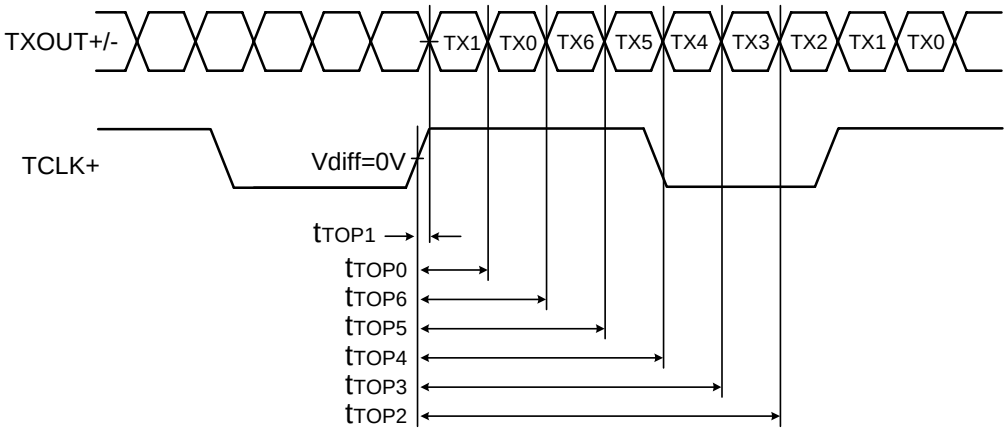


FIGURE 6. Transmitter Device Operation



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) – (TCLK-)**

FIGURE 7. Parallel TTL Data Inputs Mapped to LVDS Outputs – DTC33LM85AL

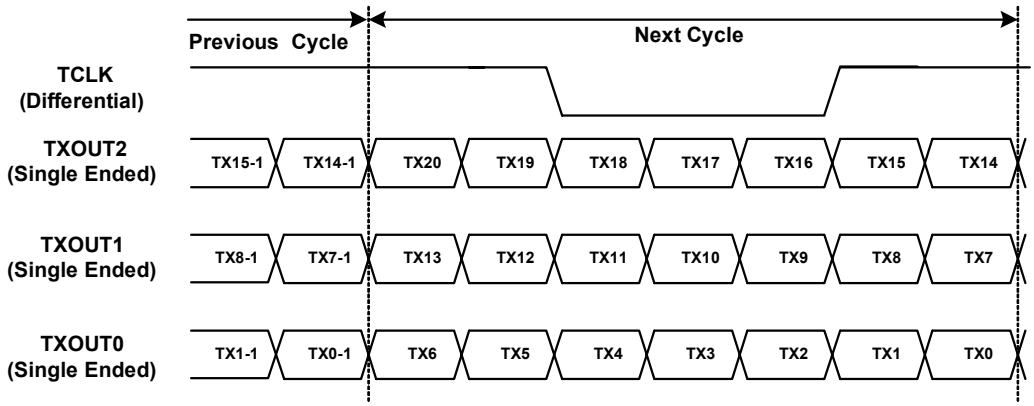
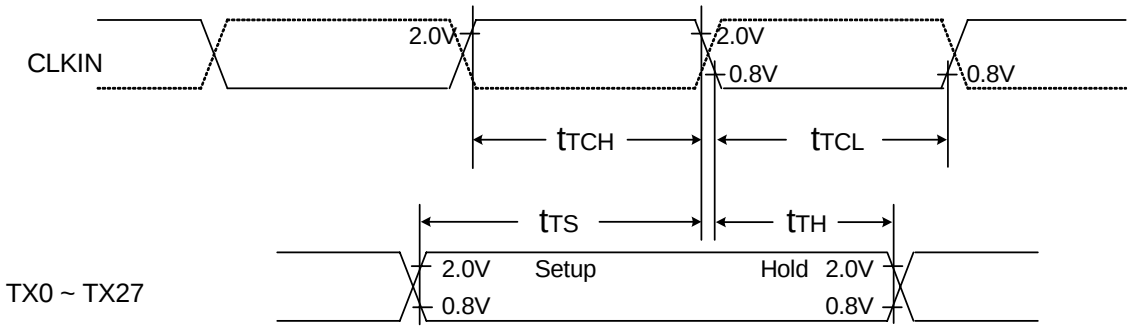


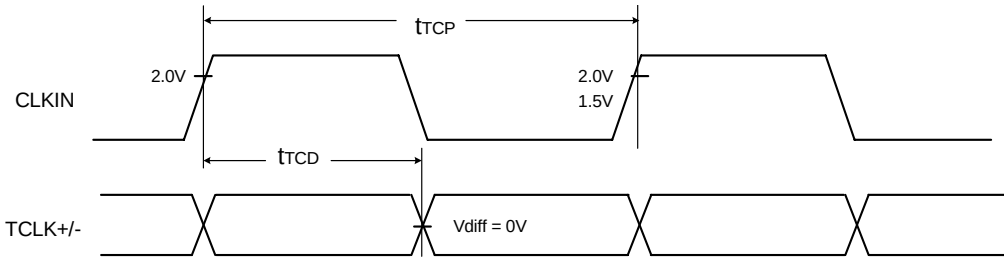
FIGURE 8. Setup/Hold and High/Low Times



Note : **1) CLKIN : for DTC33LM85AL(R/FB=GND), denoted as solid line**

for DTC33LM85AL(R/FB=VCC), denoted as dotted line

FIGURE 9. CLKIN to CLKOUT Delay



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) - (TCLK-)**

FIGURE 10. Package Pin Description

Pin Name	Pin #	Type	Description
TXOUT0-, TXOUT0+	40, 41	LVDS OUT	LVDS differential data outputs.
TXOUT1-, TXOUT1+	38, 39	LVDS OUT	
TXOUT2-, TXOUT2+	34, 35	LVDS OUT	
TCLK+, TCLK-	32, 33	LVDS OUT	LVDS differential clock outputs.
TX0 ~ TX6	44,45,47,48,1,3,4	IN	TTL level data inputs. This includes : 6 Red, 6 Green, 6 Blue, and 3 control lines (HSYNC, VSYNC, DE)
TX7 ~ TX13	6,7,9,10,12,13,15	IN	
TX14 ~ TX20	16,18,19,20,22,23,25	IN	
CLK IN	26	IN	TTL level clock input. This falling edge acts as data strobe
/PDN	27	IN	TTL level input. H : Normal operation L : Power down (all output are low)
R_FB	14	IN	Programmable strobe select. H:RIsing edge, L :Falling edge
VCC	2,8,21	Power	Power supply pins for TTL inputs.
GND	5,11,17,24,46	Ground	Ground pins for TTL inputs.
LVDS VCC	37	Power	Power supply pin for LVDS outputs.
LVDS GND	36,42	Ground	Ground pins for LVDS outputs.
PLL VCC	29	Power	Power supply pin for PLL.
PLL GND	28,30	Ground	Ground pins for PLL.

IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.

DOESTEK Co., Ltd. (www.doestek.co.kr)

6F TechnoComplex Korea Univ., Anam-Dong5-Ga, Songbuk-Gu, SEOUL, KOREA Tel) 82-2-926-9464