LVDS Product

DTC30LM36 *(Rev. 1.1)*

REVISED AUGUST 2008

+3.3V LVDS 60Bit Flat Panel Display (FPD) Receiver – 135MHz

General Description

The DTC30LM36 receiver is designed to support Dual/Single link transmissions between Host and Flat Panel Display up to 1080p and QXGA resolutions. It receives and converts LVDS (Low Voltage Differential Signal) data streams back into 67 bits of CMOS/TTL data with either falling edge or rising edge clock for convenient interface with a variety of LCD panel controllers.

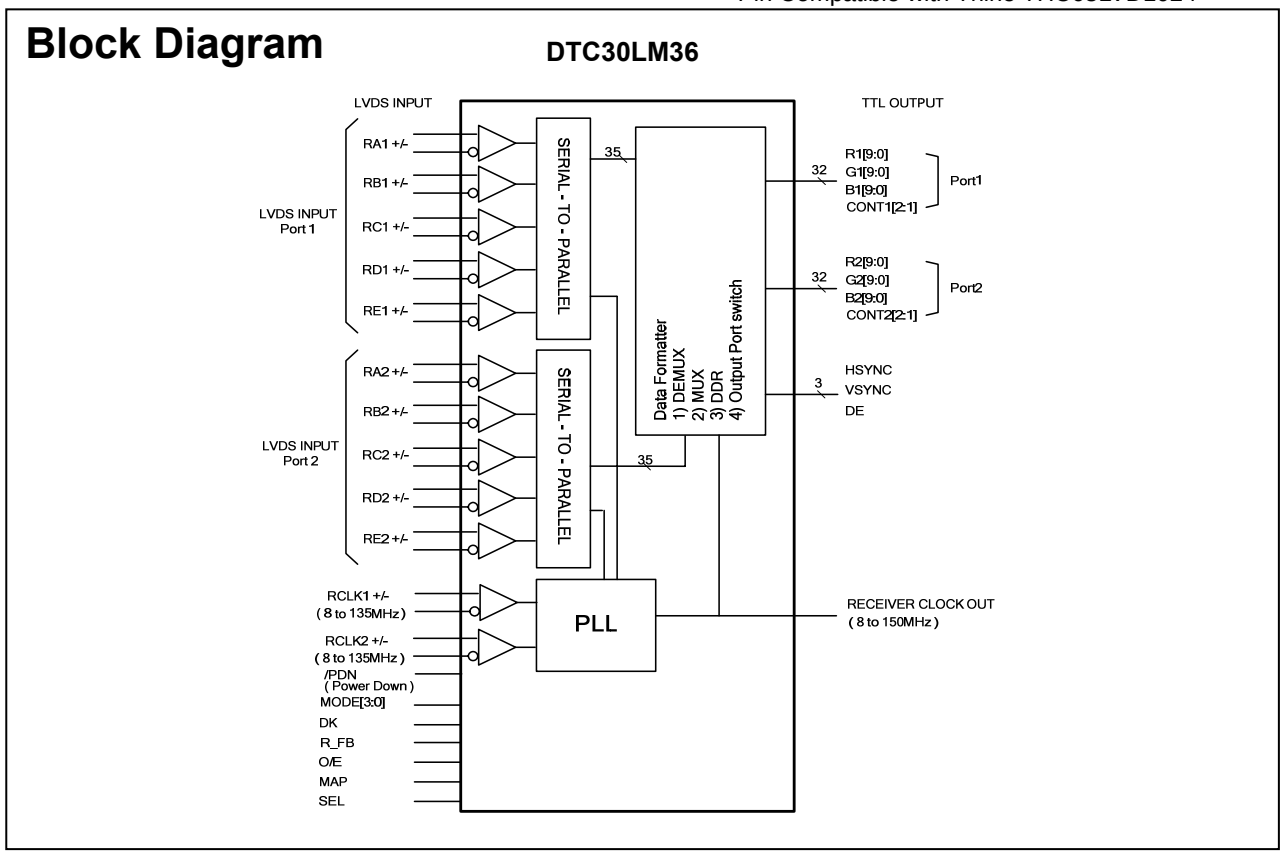
When using a 135 MHz clock and dual link transmission, the data throughput is 1.1 Gbytes/sec with an effective data rate of 945 Mbps per LVDS channel. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

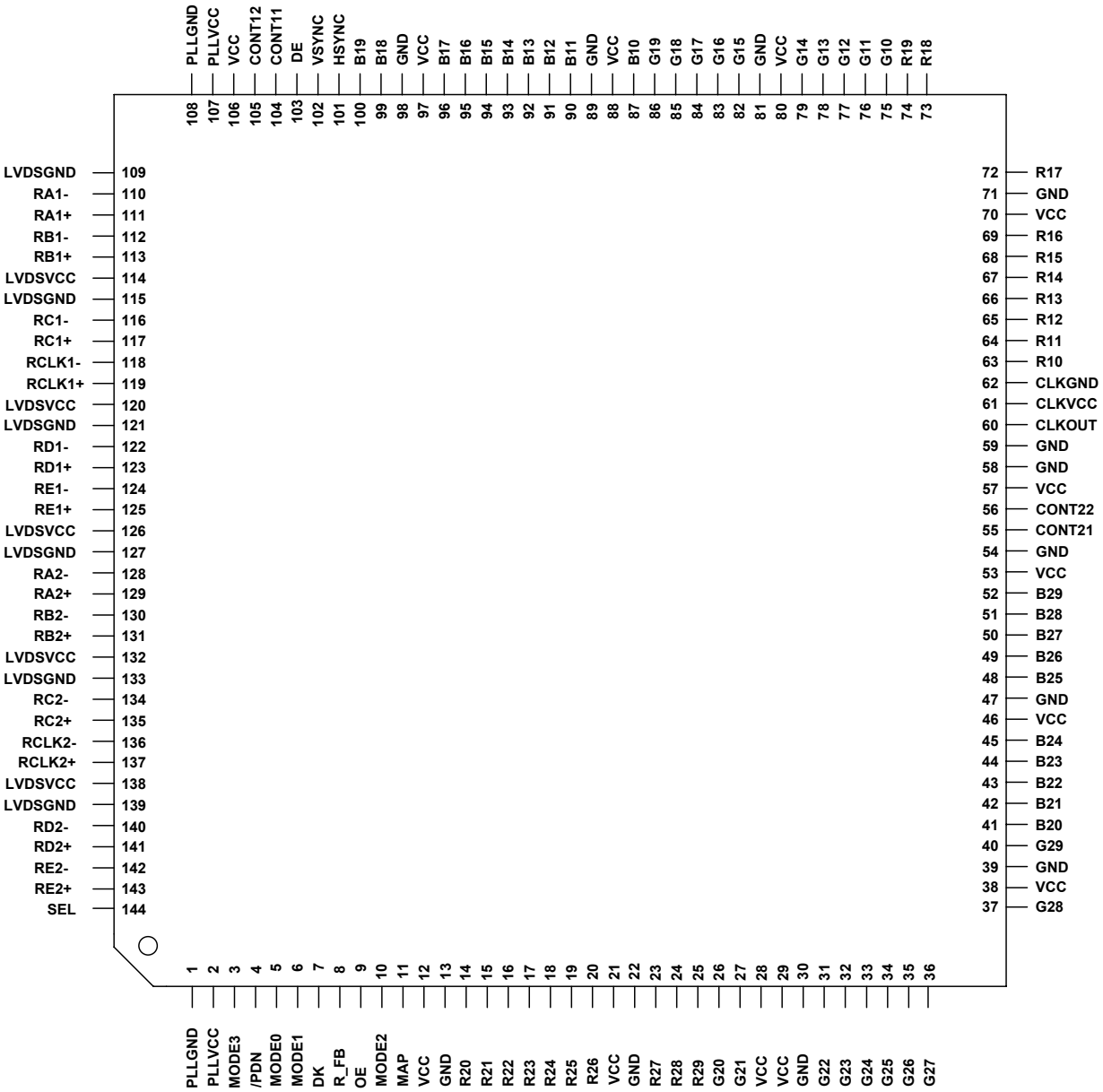
- Wide frequency range
  Dual IN / Dual Out Mode: 8 -135MHz (CLKOUT)
  Dual IN / Single Out Mode: 40 -150MHz (CLKOUT)
- Supports 480i ~ 1080p and VGA ~QXGA
- Power down mode
- Single 3.3V supply
- PLL requires No external components
- Flexible Input/Output Options
  1. Single/Dual LVDS port IN, Single/Dual TTL port OUT
  2. Double Clock Edge output option
  3. Output Port Switch
  4. 1 or 2 Clock input option
- TTL clock edge selectable
- Flexible TTL clock output offset
- 2 Output data mapping for simplifying PCB layout
- 144 pin LQFP Package
- Pin Compatible with Thine THC63LVD1024

Block Diagram

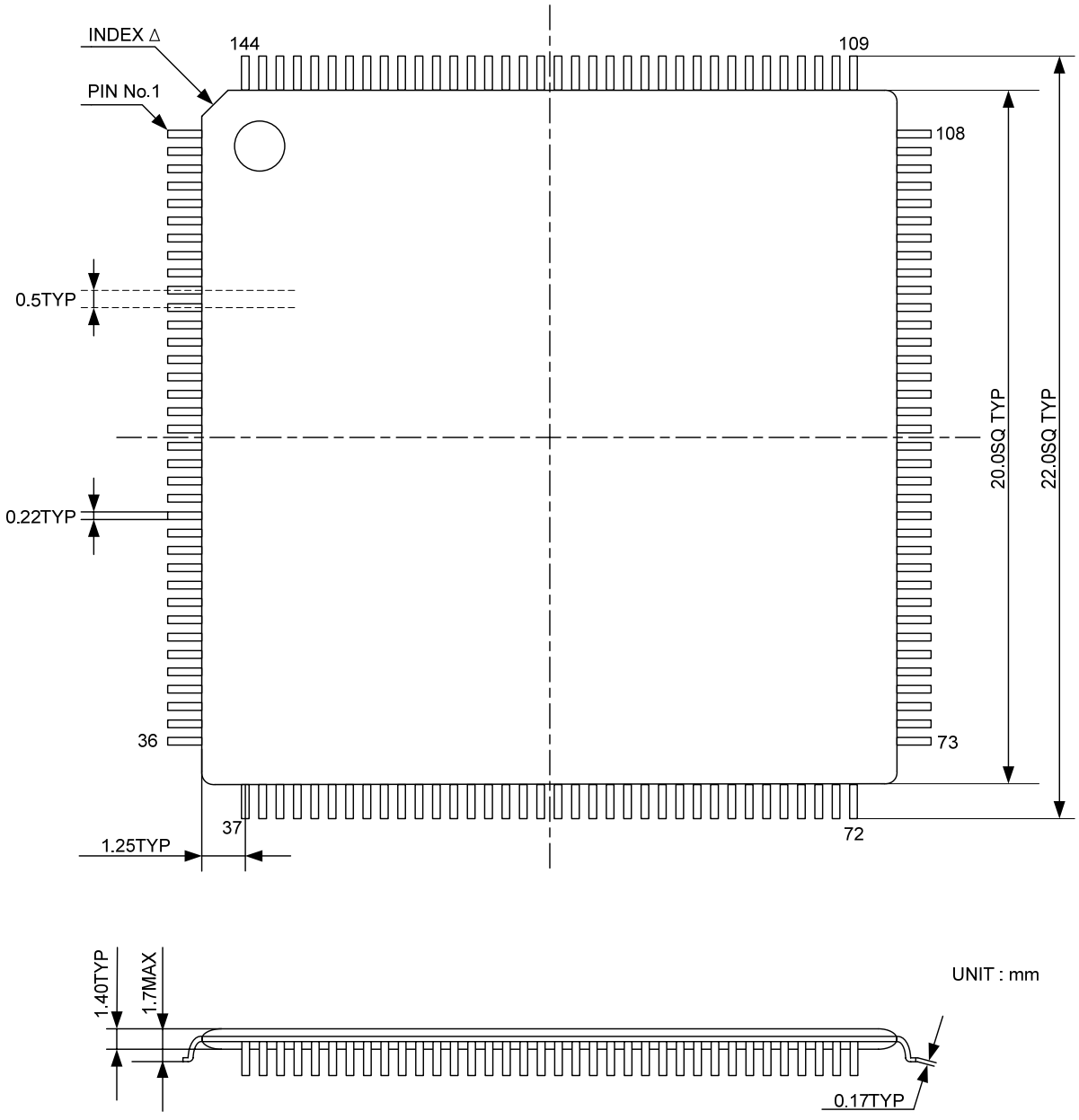
DTC30LM36



PIN OUT


108 PLLGND
107 PLLVCC
106 VCC
105 CONT12
104 CONT11
103 DE
102 VSYNC
101 HSYNC
100 B19
99 B18
98 GND
97 VCC
96 B17
95 B16
94 B15
93 B14
92 B13
91 B12
90 B11
89 GND
88 VCC
87 B10
86 G19
85 G18
84 G17
83 G16
82 G15
81 GND
80 VCC
79 G14
78 G13
77 G12
76 G11
75 G10
74 R19
73 R18
109 LVDSGND
110 RA1-
111 RA1+
112 RB1-
113 RB1+
114 LVDSVCC
115 LVDSGND
116 RC1-
117 RC1+
118 RCLK1-
119 RCLK1+
120 LVDSVCC
121 LVDSGND
122 RD1-
123 RD1+
124 RE1-
125 RE1+
126 LVDSVCC
127 LVDSGND
128 RA2-
129 RA2+
130 RB2-
131 RB2+
132 LVDSVCC
133 LVDSGND
134 RC2-
135 RC2+
136 RCLK2-
137 RCLK2+
138 LVDSVCC
139 LVDSGND
140 RD2-
141 RD2+
142 RE2-
143 RE2+
144 SEL
72 R17
71 GND
70 VCC
69 R16
68 R15
67 R14
66 R13
65 R12
64 R11
63 R10
62 CLKGND
61 CLKVCC
60 CLKOUT
59 GND
58 GND
57 VCC
56 CONT22
55 CONT21
54 GND
53 VCC
52 B29
51 B28
50 B27
49 B26
48 B25
47 GND
46 VCC
45 B24
44 B23
43 B22
42 B21
41 B20
40 G29
39 GND
38 VCC
37 G28
1 PLLGND
2 PLLVCC
3 MODE3
4 /PDN
5 MODE0
6 MODE1
7 DK
8 R_FB
9 OE
10 MODE2
11 MAP
12 VCC
13 GND
14 R20
15 R21
16 R22
17 R23
18 R24
19 R25
20 R26
21 VCC
22 GND
23 R27
24 R28
25 R29
26 G20
27 G21
28 VCC
29 VCC
30 GND
31 G22
32 G23
33 G24
34 G25
35 G26
36 G27

PACKAGE


INDEX △
144
109
PIN No.1
108
0.5TYP
20.0SQ TYP
22.0SQ TYP
0.22TYP
36
73
37
72
1.25TYP
1.40TYP
1.7MAX
UNIT : mm
0.17TYP

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>RA1+ , RA1-</td><td>111,110</td><td rowspan="5">LVDS IN</td><td rowspan="5">1st Link.
1st Pixel input data in Dual-Link Input Mode option.</td></tr>
<tr><td>RB1+ , RB1-</td><td>113,112</td></tr>
<tr><td>RC1+ , RC1-</td><td>117,116</td></tr>
<tr><td>RD1+ , RD1-</td><td>123,122</td></tr>
<tr><td>RE1+ , RE1-</td><td>125,124</td></tr>
<tr><td>RCLK1+ , RCLK1-</td><td>119,118</td><td>LVDS IN</td><td>1st Link. LVDS Clock input.</td></tr>
<tr><td>RA2+ , RA2-</td><td>129,128</td><td rowspan="5">LVDS IN</td><td rowspan="5">2nd Link.
2nd Pixel input data in Dual-Link Input Mode option.</td></tr>
<tr><td>RB2+ , RB2-</td><td>131,130</td></tr>
<tr><td>RC2+ , RC2-</td><td>135,134</td></tr>
<tr><td>RD2+ , RD2-</td><td>141,140</td></tr>
<tr><td>RE2+ , RE2-</td><td>143,142</td></tr>
<tr><td>RCLK2+ , RCLK2-</td><td>137,136</td><td>LVDS IN</td><td>2nd Link. LVDS Clock input.</td></tr>
<tr><td>R19~R10</td><td>74 - 72, 69 - 63</td><td rowspan="3">OUT</td><td rowspan="3">1st Pixel, TTL level Data Outputs.</td></tr>
<tr><td>G19~G10</td><td>86 - 82, 79 - 75</td></tr>
<tr><td>B19~B10</td><td>100, 99,
96 - 90, 87</td></tr>
<tr><td>R29~R20</td><td>25 - 23, 20 - 14</td><td rowspan="3">OUT</td><td rowspan="3">2nd Pixel, TTL level Data Outputs.</td></tr>
<tr><td>G29~G20</td><td>40, 37 - 31,
27, 26</td></tr>
<tr><td>B29~B20</td><td>52 - 48, 45 - 41</td></tr>
<tr><td>CONT11,CONT12</td><td>104, 105</td><td rowspan="2">OUT</td><td rowspan="2">TTL level Control Data Outputs.</td></tr>
<tr><td>CONT21,CONT22</td><td>55, 56</td></tr>
<tr><td>DE</td><td>103</td><td>OUT</td><td>TTL level Data Enable Output.</td></tr>
<tr><td>VSYNC</td><td>102</td><td>OUT</td><td>TTL level Vsync Output.</td></tr>
<tr><td>HSYNC</td><td>101</td><td>OUT</td><td>TTL level Hsync Output.</td></tr>
<tr><td>CLKOUT</td><td>60</td><td>OUT</td><td>TTL level Clock Output.</td></tr>
<tr><td>/PDN</td><td>4</td><td>IN</td><td>Power down and Output Control.(Table1)
H: Normal operation
L: Power down</td></tr>
<tr><td>MODE1,MODE0</td><td>6,5</td><td>IN</td><td>Pixel Data Mode
<table>
<tr><th>Mode1</th><th>Mode0</th><th>Mode</th></tr>
<tr><td>H</td><td>H</td><td>Single Link(Single-in/Single-Out)</td></tr>
<tr><td>H</td><td>L</td><td>Single Link(Single-in/Dual-Out)</td></tr>
<tr><td>L</td><td>H</td><td>Dual Link (Dual-in/Single-Out)</td></tr>
<tr><td>L</td><td>L</td><td>Dual Link (Dual-in/Dual-Out)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>DK</td><td>7</td><td>IN</td><td>Output Clock Delay Timing Select Option.
<table>
<tr><th>MODE[1:0]</th><th>DK</th><th>Offset</th></tr>
<tr><td rowspan="3">X</td><td>L</td><td>0</td></tr>
<tr><td>M</td><td>$-\frac{6}{28}t_{DOUT}$</td></tr>
<tr><td>H</td><td>$+\frac{6}{28}t_{DOUT}$</td></tr>
</table>
t_{DOUT} = Output Data Cycle</td></tr>
<tr><td>R_FB</td><td>8</td><td>IN</td><td>Output Clock Triggering Edge Select.
H : Rising edge L : Falling edge</td></tr>
<tr><td>OE</td><td>9</td><td>IN</td><td>Output Enable Option.(Table1)
H : Output enable L : Output disable</td></tr>
<tr><td>MODE2</td><td>10</td><td>IN</td><td>DDR function Enable Option.
The use of this function depends on the setting of MODE<1:0> :
MODE<1:0>=LH(Dual-in/Single-out Mode)
H: DDR(Double Edge Output) function enable.
L: DDR(Double Edge Output) function disable.
MODE<1:0>=Other
Must be tied to GND</td></tr>
<tr><td>MAP</td><td>11</td><td>IN</td><td>LVDS mapping table select.(See Fig 11, 12 and Tables 2~ 9)
H : Mapping Mode1
L : Mapping Mode2</td></tr>
<tr><td>MODE3</td><td>3</td><td>IN</td><td>Output Port Switch Option.
The use of this function depends on the setting of MODE<1:0> :
MODE<1:0>=LH(Dual-in/Single-out Mode)
H : Port Switch Disable
L : Port Switch Enable</td></tr>
<tr><td>SEL</td><td>144</td><td>IN</td><td>LVDS 2nd Port Clock input control option
H or Open : 2nd Port Clock Enable.
L : 2nd Port Clock Disable.</td></tr>
<tr><td>VCC</td><td>12, 21, 28, 29, 38, 46, 53, 57, 70, 80, 88, 97, 106</td><td>Power</td><td>Power Supply Pins for TTL inputs and digital circuitry.</td></tr>
<tr><td>GND</td><td>13, 22, 30, 39, 47, 54, 58, 59, 71, 81, 89, 98</td><td>Ground</td><td>Ground Pins of TTL inputs and digital circuitry.</td></tr>
<tr><td>LVDSVCC</td><td>114, 120, 126, 132, 138</td><td>Power</td><td>Power Supply Pins for LVDS Inputs.</td></tr>
<tr><td>LVDSGND</td><td>109, 115, 121, 127, 133, 139</td><td>Ground</td><td>Ground Pins for LVDS Inputs.</td></tr>
<tr><td>PLLVCC</td><td>2, 107</td><td>Power</td><td>Power Supply Pins for PLL circuitry.</td></tr>
<tr><td>PLLGND</td><td>1, 108</td><td>Ground</td><td>Ground Pins for PLL circuitry.</td></tr>
<tr><td>CLKVCC</td><td>61</td><td>Power</td><td>Power Supply Pins for TTL output of CLKOUT.</td></tr>
<tr><td>CLKGND</td><td>62</td><td>Ground</td><td>Ground Pins for TTL output of CLKOUT.</td></tr>
</table>

Absolute Maximum Ratings

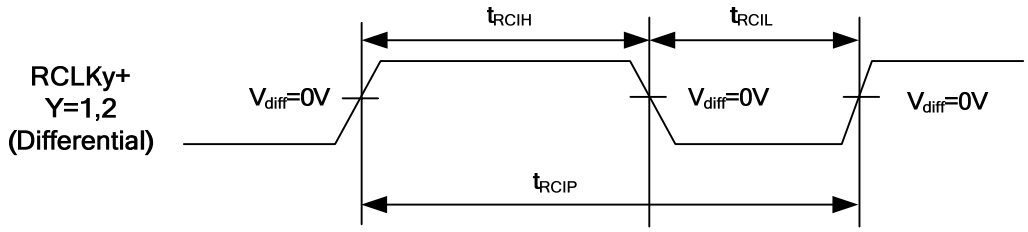
Supply voltage (V_{CC})	**-0.3V ~ +4.0V**
CMOS / TTL Input Voltage.	**-0.3V ~ (V_{CC} + 0.3V)**
LVDS Driver Output Voltage.	**-0.3V ~ (V_{CC} + 0.3V)**
Output Current.	**-30mA ~ 30mA**
Junction Temperature.	**+125°C**
Storage Temperature Range.	**-55°C ~ 125°C**
Lead Temperature (Soldering, 4sec)	**+260°C**
Maximum Power Dissipation	**2.5W**

Note: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

Parameter				Min	Typ	Max	Units
All Supply Voltage				3.0	3.3	3.6	V
Operating Ambient Temperature				-10		70	°C
Clock Frequency	MODE<1:0> = LL Dual-in / Dual-out		LVDS Input	8		135	MHz
			Output	8		135	MHz
	MODE<1:0> = LH Dual-in / Single-out	Single Edge Output (MODE2 = L)	LVDS Input	20		75	MHz
			Output	40		150	MHz
		Double Edge Output (MODE2 = H)	LVDS Input	20		75	MHz
			Output	20		75	MHz
	MODE<1:0> = HL Single-in / Dual-out		LVDS Input	8		135	MHz
			Output	4		67.5	MHz
	MODE<1:0> = HH Single-in / Single-out		LVDS Input	8		135	MHz
			Output	8		135	MHz
Differential CLKIN High Time(t_{RCIH})(Fig1)				$2\frac{t_{RCIP}}{7}$		$5\frac{t_{RCIP}}{7}$	nS
Differential CLKIN Low Time(t_{RCIL})(Fig1)				$2\frac{t_{RCIP}}{7}$		$5\frac{t_{RCIP}}{7}$	nS

Figure 1. Differential CLKIN



Electrical Characteristics

CMOS / TTL DC SPECIFICATIONS

V_{CC} = VCC=PLLVCC=LVDSVCC=CLKVCC

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	/PDN, MODE[3:0], R_FB, OE, MAP	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{IH3}	High Level Input Voltage	3-Level Inputs(DK Pin)	0.8 V_{CC}		V_{CC}	V
V_{IM3}	Middle Level Input Voltage		0.4 V_{CC}		0.6 V_{CC}	V
V_{IL3}	Low Level Input Voltage		GND		0.2 V_{CC}	V
V_{OH}	High Level Output Voltage	I_{OH} = -8mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 8mA			0.4	V
I_{IN}	Input Current	GND ≤ V_{IN} ≤ V_{CC}			±10	μA
I_{IL3}	3-Level Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}			±10	μA

LVDS Receiver DC Specifications

V_{CC} = VCC=PLLVCC=LVDSVCC=CLKVCC

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{IC} = 1.2V			100	mV
V_{TL}	Differential Input Low Threshold	V_{IC} = 1.2V	-100			mV
I_{IN}	Input Current	V_{IN} = 2.4V / 0V			±10	μA

Electrical Characteristics (Continued)

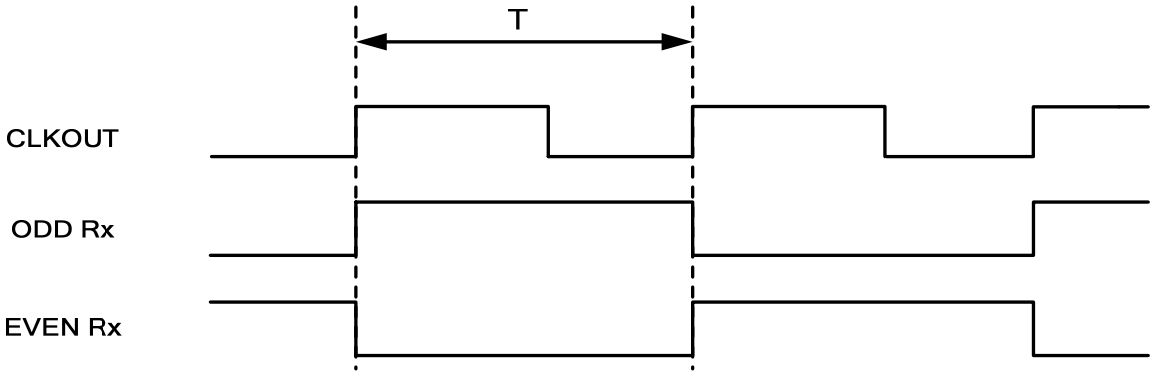
SUPPLY CURRENT

V_{CC} = VCC=PLLVCC=LVDSVCC=CLKVCC

Symbol	Parameter	Conditions			Typ	Max	Units
I_{RCCW}	Receiver Supply Current (Worst Case Pattern) Fig2.	CL = 8pF	MODE<1:0> = HH Single-in/Single-out MODE2 = L	CLKOUT=65MHz		139	mA
				CLKOUT=85MHz		172	mA
				CLKOUT=135MHz		252	mA
			MODE<1:0> = HL Single-in/Dual-out	CLKOUT=32.5MHz		127	mA
				CLKOUT=42.5MHz		155	mA
				CLKOUT=67.5MHz		226	mA
			MODE<1:0> = LH Dual-in/Single out MODE2 = L, MODE3 = H DDR Output Off (SEL = L)	CLKOUT=65MHz		148	mA
				CLKOUT=85MHz		174	mA
				CLKOUT=135MHz		242	mA
				CLKOUT=150MHz		263	mA
			MODE<1:0> = LH Dual-in/ Single-out MODE2 = H, MODE3 = H DDR Output On (SEL = L)	CLKOUT=32.5MHz		141	mA
				CLKOUT=42.5MHz		166	mA
				CLKOUT=67.5MHz		231	mA
				CLKOUT=75MHz		251	mA
			MODE<1:0> = LL Dual-in/Dual-out (SEL = L)	CLKOUT=65MHz		242	mA
				CLKOUT=85MHz		299	mA
				CLKOUT=135MHz		442	mA
I_{RCCS}	Receiver Power Down Supply Current	/PDN = L				50	µA

*

Figure 2. "Worst case pattern"



Switching Characteristics

V_{CC} = VCC=PLLVCC=LVDSVCC=CLKVCC

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{RCP}	CLKOUT Period (Fig 4)		6.67	T	250	ns
t_{RCH}	CLKOUT High Time (Fig 4)			$\frac{T}{2}$		ns
t_{RCL}	CLKOUT Low Time (Fig 4)			$\frac{T}{2}$		ns
t_{DOUT}	TTL Data OUT Period (Fig 5,6)		6.67	T	250	ns
t_{RS}	TTL Data Setup to CLKOUT (Fig 5,6)		$0.45t_{RCP}$-0.45			ns
t_{RH}	TTL Data Hold to CLKOUT (Fig 5,6)		$0.45t_{RCP}$-0.45			ns
t_{TLH}	TTL Low to High Transition Time (Fig 3)			0.7	1.0	ns
t_{THL}	TTL High to Low Transition Time (Fig 3)			0.7	1.0	ns
t_{RCIP}	CLKIN Period (Fig 1)		7.4		125.0	ns
t_{SK}	Receiver Skew Margin (Fig 7)	t_{RCIP} = 85MHz	-450	0	450	ps
t_{RIP1}	Input Data Position 0 (Fig 7)		$-t_{SK}$	0	$+t_{SK}$	ps
t_{RIP0}	Input Data Position 1 (Fig 7)		$\frac{t_{RCIP}}{7}-t_{SK}$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}+t_{SK}$	ns
t_{RIP6}	Input Data Position 2 (Fig 7)		$2\frac{t_{RCIP}}{7}-t_{SK}$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}+t_{SK}$	ns
t_{RIP5}	Input Data Position 3 (Fig 7)		$3\frac{t_{RCIP}}{7}-t_{SK}$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}+t_{SK}$	ns
t_{RIP4}	Input Data Position 4 (Fig 7)		$4\frac{t_{RCIP}}{7}-t_{SK}$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}+t_{SK}$	ns
t_{RIP3}	Input Data Position 5 (Fig 7)		$5\frac{t_{RCIP}}{7}-t_{SK}$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}+t_{SK}$	ns
t_{RIP2}	Input Data Position 6 (Fig 7)		$6\frac{t_{RCIP}}{7}-t_{SK}$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}+t_{SK}$	ns
t_{RPLL}	PLL Lock Set Time (Fig 8)				10.0	ms
t_{RCD}	RCLK +/- to CLKOUT Delay (Fig 9) MODE<1:0>=LL, Dual-in, Dual-out			$4t_{RCIP}$+8.3ns		ns
t_{DEINT}	MODE<1:0>=HL (Single IN/Dual OUT Mode) Only	DE input period (Fig 10)	$4t_{RCIP}$	t_{RCIP}*(2n) n=integer		ns
t_{DEH}		DE input High time (Fig 10)	$2t_{RCIP}$			ns
t_{DEL}		DE input Low time (Fig 10)	$2t_{RCIP}$			ns

AC Timing Diagrams

Figure 3. CMOS/TTL Output Load and Transition Time

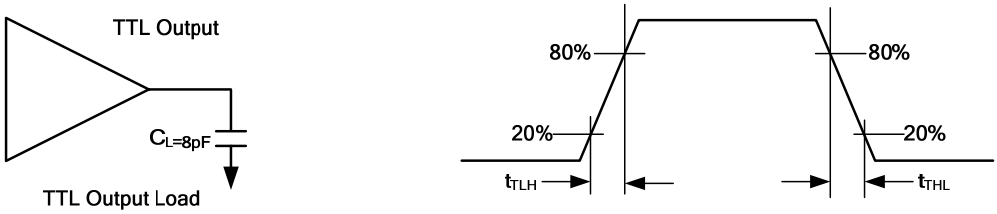


Figure 4. CLKOUT Period and High/Low Time

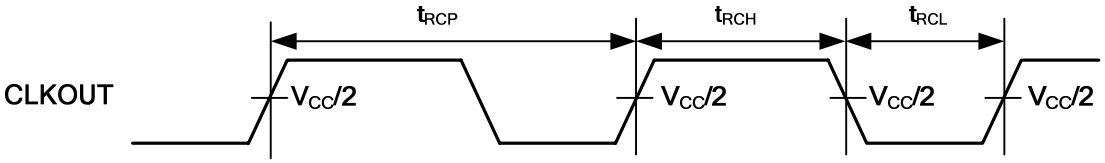


Figure 5. CLKOUT Position and Setup/Hold Timing

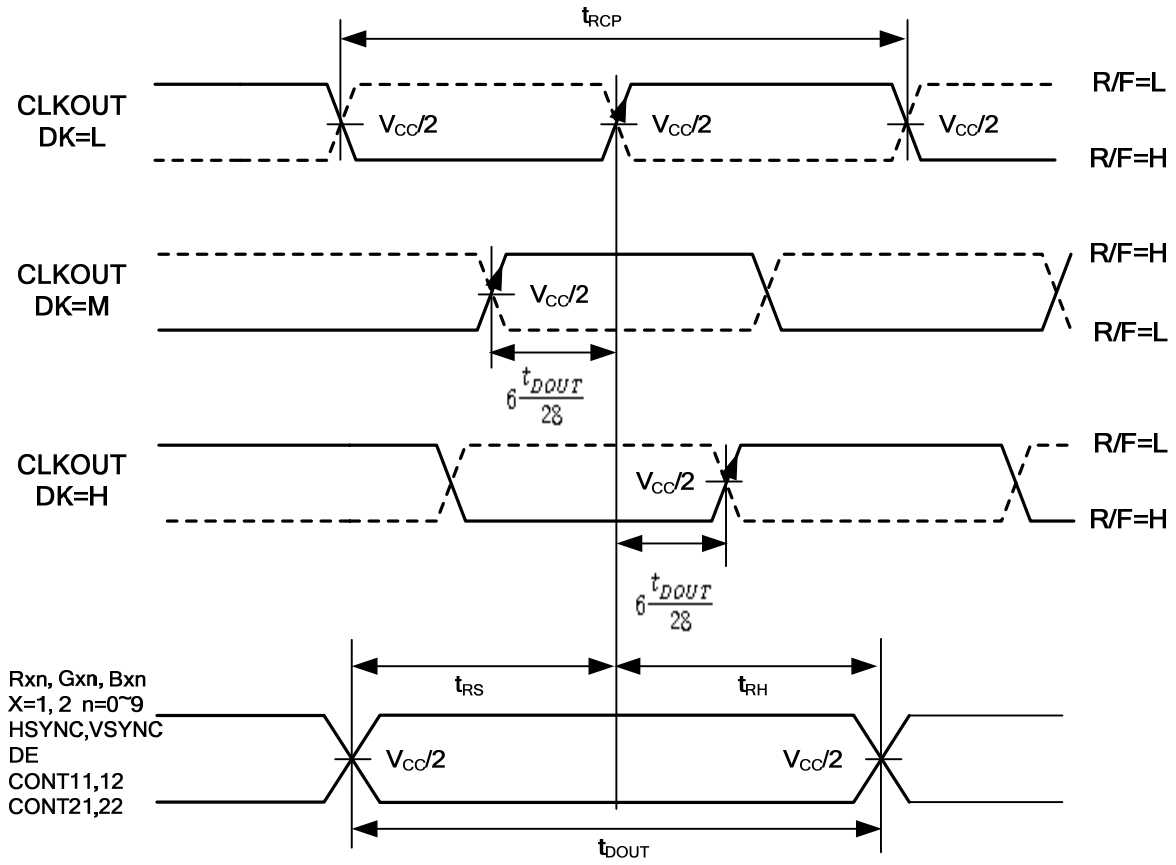


Figure 6. CLKOUT Position and Setup/Hold Timing for Double Edge Output Mode
MODE<1:0>=LH, MODE2=H

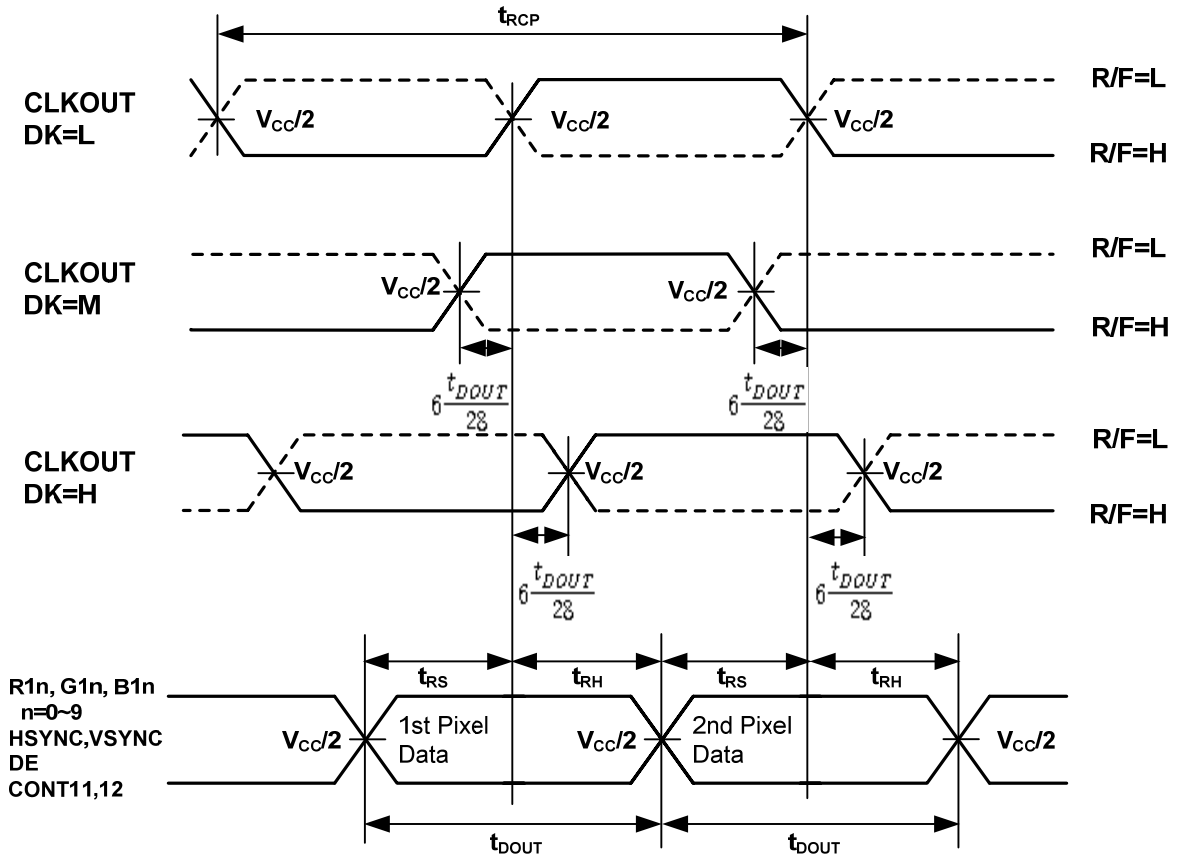
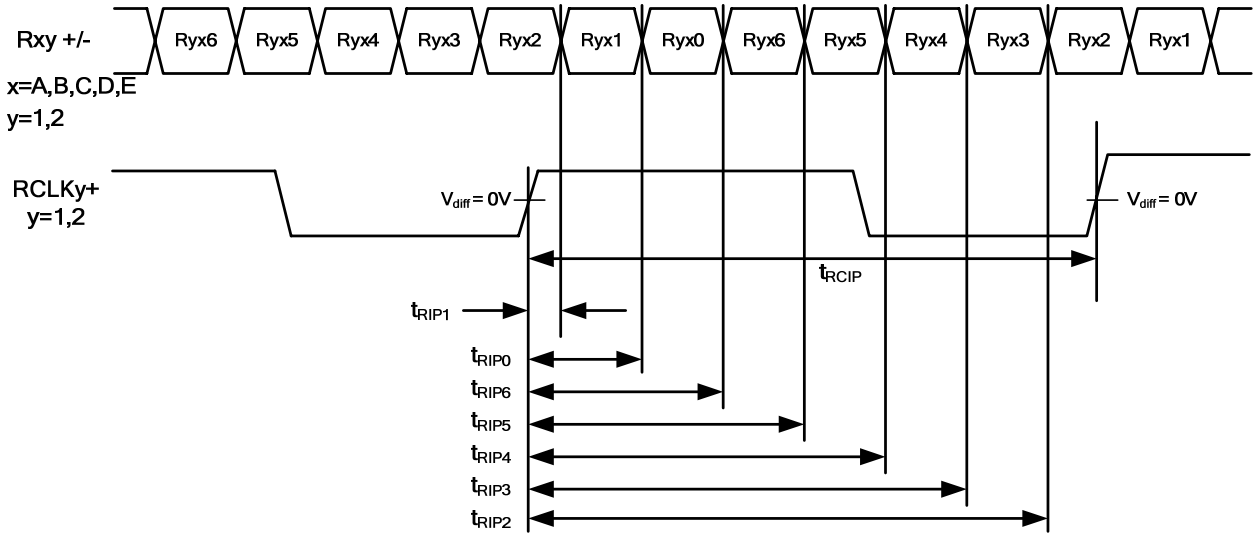


Figure 7. LVDS Input Data Position



Note: 1) V_{diff} = (Ryx+) – (Ryx-), …….. (RCLKy+) – (RCLKy-)

Figure 8. PLL Lock Set Time

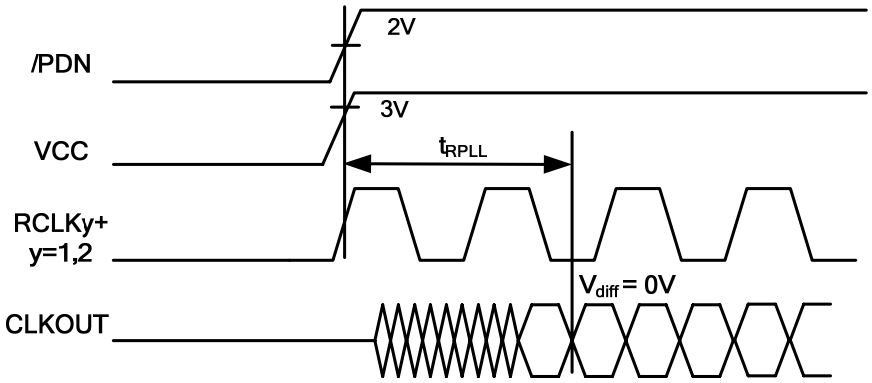


Figure 9. RCLK to CLKOUT delay (Latency)

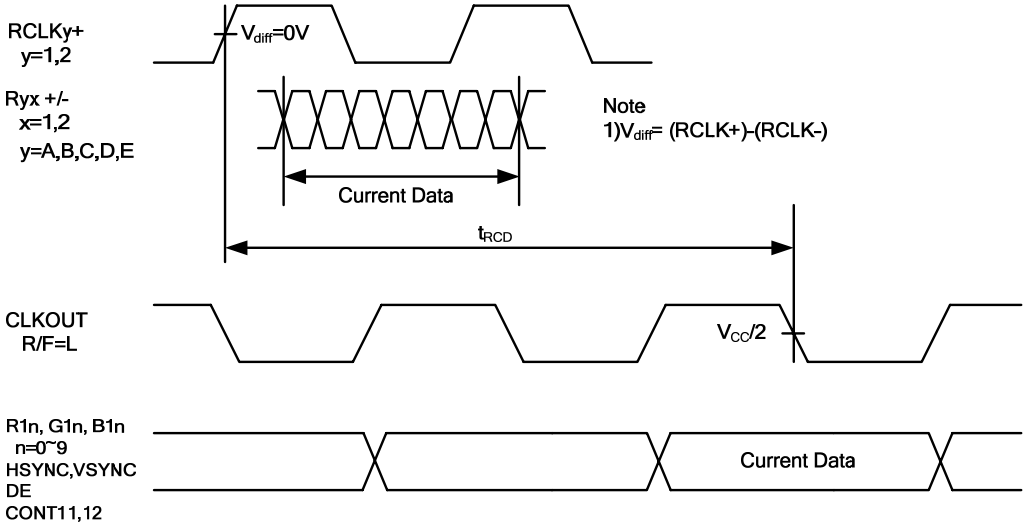
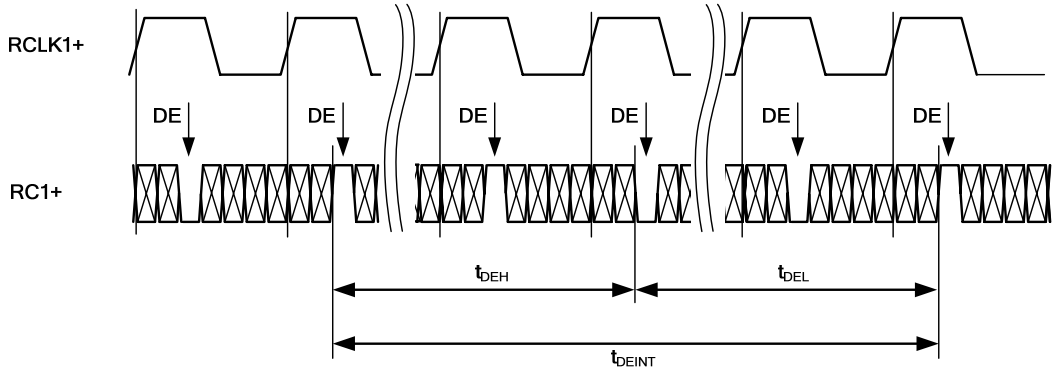


Figure 10. DE Input Timing for Single In, Dual Out Mode Option



Power Down and Output Enable Control

Table 1 : Output Control

/PDN	R_FB	OE	Data Outputs	Clock Outputs
0	0	0	Hi-Z	Hi-Z
0	0	1	All 0	Fixed Low
0	1	0	Hi-Z	Hi-Z
0	1	1	All 0	Fixed Low
1	0	0	Hi-Z	Hi-Z
1	0	1	Data Out	Negative Clock
1	1	0	Hi-Z	Hi-Z
1	1	1	Data Out	Positive Clock

Output Data Mapping

Table 2 : Output Color Data naming rule

X	Y	Z	Description	
X = R			Red Color Data	
X = G			Green Color Data	
X = B			Blue Color Data	
	Y = None		Single Pixel	
	Y = O		Dual Pixel	1’st Pixel Data
	Y = E			2’nd Pixel Data
		Z = 0 ~ 9	Bit number 0 : LSB (Least significant Bit) 9 : MSB (Most Significant Bit)	

Output Data Mapping (Continued)

Table 3 : TTL / CMOS Output Data Mapping (Single-out mode, MODE0 = H)

Data Signals			Receiver Output Pin Names		
30 Bit	24 Bit	18 Bit	30 Bit	24 Bit	18 Bit
R0			R10		
R1			R11		
R2	R0		R12	R12	
R3	R1		R13	R13	
R4	R2	R0	R14	R14	R14
R5	R3	R1	R15	R15	R15
R6	R4	R2	R16	R16	R16
R7	R5	R3	R17	R17	R17
R8	R6	R4	R18	R18	R18
R9	R7	R5	R19	R19	R19
G0			G10		
G1			G11		
G2	G0		G12	G12	
G3	G1		G13	G13	
G4	G2	G0	G14	G14	G14
G5	G3	G1	G15	G15	G15
G6	G4	G2	G16	G16	G16
G7	G5	G3	G17	G17	G17
G8	G6	G4	G18	G18	G18
G9	G7	G5	G19	G19	G19
B0			B10		
B1			B11		
B2	B0		B12	B12	
B3	B1		B13	B13	
B4	B2	B0	B14	B14	B14
B5	B3	B1	B15	B15	B15
B6	B4	B2	B16	B16	B16
B7	B5	B3	B17	B17	B17
B8	B6	B4	B18	B18	B18
B9	B7	B5	B19	B19	B19

Output Data Mapping (Continued)

Table 4 : TTL / CMOS Output Data Mapping (Dual-out Mode, MODE0 = L)

1'st Pixel Data						2'nd Pixel Data					
Data Signals			Receiver Output Pin Names			Data Signals			Receiver Output Pin Names		
30 Bit	24 Bit	18 Bit	30 Bit	24 Bit	18 Bit	30 Bit	24 Bit	18 Bit	30 Bit	24 Bit	18 Bit
RE0			R10			RO0			R20		
RE1			R11			RO1			R21		
RE2	RE0		R12	R12		RO2	RO0		R22	R22	
RE3	RE1		R13	R13		RO3	RO1		R23	R23	
RE4	RE2	RE0	R14	R14	R14	RO4	RO2	RO0	R24	R24	R24
RE5	RE3	RE1	R15	R15	R15	RO5	RO3	RO1	R25	R25	R25
RE6	RE4	RE2	R16	R16	R16	RO6	RO4	RO2	R26	R26	R26
RE7	RE5	RE3	R17	R17	R17	RO7	RO5	RO3	R27	R27	R27
RE8	RE6	RE4	R18	R18	R18	RO8	RO6	RO4	R28	R28	R28
RE9	RE7	RE5	R19	R19	R19	RO9	RO7	RO5	R29	R29	R29
GE0			G10			GO0			G20		
GE1			G11			GO1			G21		
GE2	GE0		G12	G12		GO2	GO0		G22	G22	
GE3	GE1		G13	G13		GO3	GO1		G23	G23	
GE4	GE2	GE0	G14	G14	G14	GO4	GO2	GO0	G24	G24	G24
GE5	GE3	GE1	G15	G15	G15	GO5	GO3	GO1	G25	G25	G25
GE6	GE4	GE2	G16	G16	G16	GO6	GO4	GO2	G26	G26	G26
GE7	GE5	GE3	G17	G17	G17	GO7	GO5	GO3	G27	G27	G27
GE8	GE6	GE4	G18	G18	G18	GO8	GO6	GO4	G28	G28	G28
GE9	GE7	GE5	G19	G19	G19	GO9	GO7	GO5	G29	G29	G29
BE0			B10			BO0			B20		
BE1			B11			BO1			B21		
BE2	BE0		B12	B12		BO2	BO0		B22	B22	
BE3	BE1		B13	B13		BO3	BO1		B23	B23	
BE4	BE2	BE0	B14	B14	B14	BO4	BO2	BO0	B24	B24	B24
BE5	BE3	BE1	B15	B15	B15	BO5	BO3	BO1	B25	B25	B25
BE6	BE4	BE2	B16	B16	B16	BO6	BO4	BO2	B26	B26	B26
BE7	BE5	BE3	B17	B17	B17	BO7	BO5	BO3	B27	B27	B27
BE8	BE6	BE4	B18	B18	B18	BO8	BO6	BO4	B28	B28	B28
BE9	BE7	BE5	B19	B19	B19	BO9	BO7	BO5	B29	B29	B29

LVDS Input Data Mapping

Figure 11. LVDS Inputs Mapped to TTL Data Outputs
MODE1 = H (Single-in Mode)

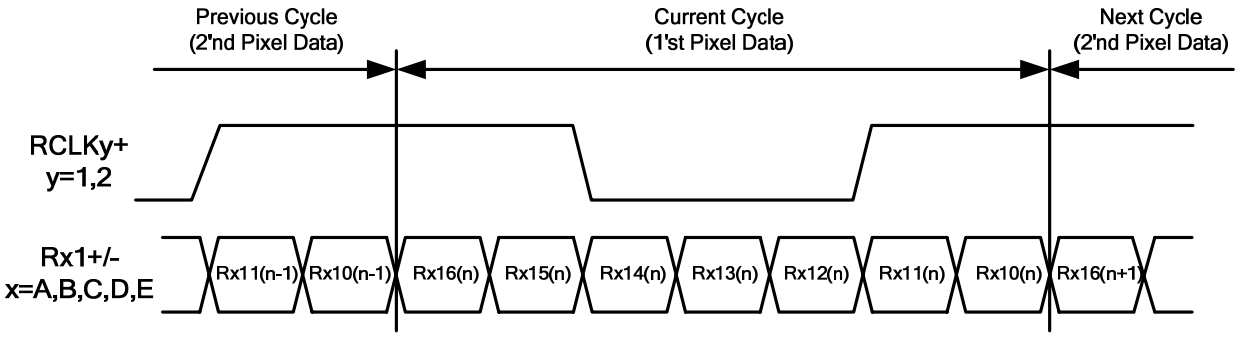


Figure 12.a. LVDS Inputs Mapped to TTL Data Outputs
MODE1 = L (Dual-in Mode) SEL = L

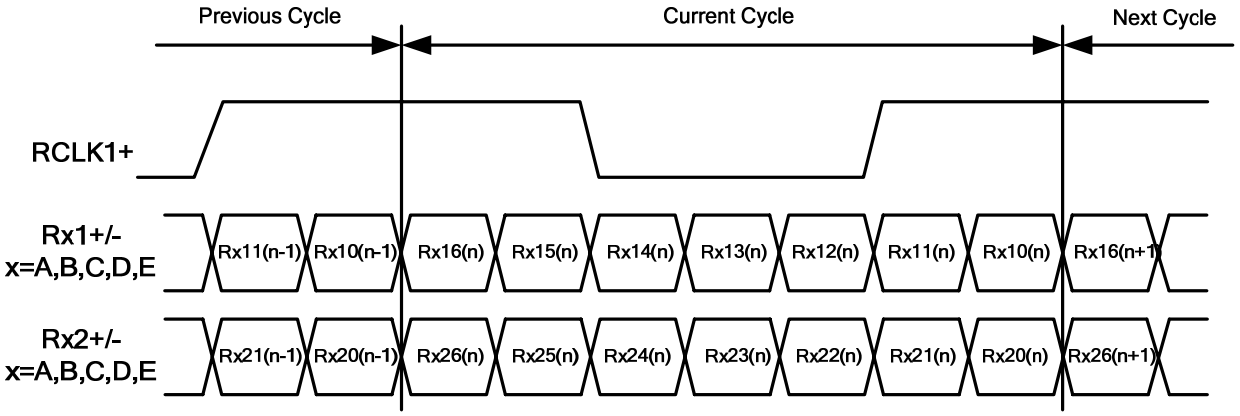
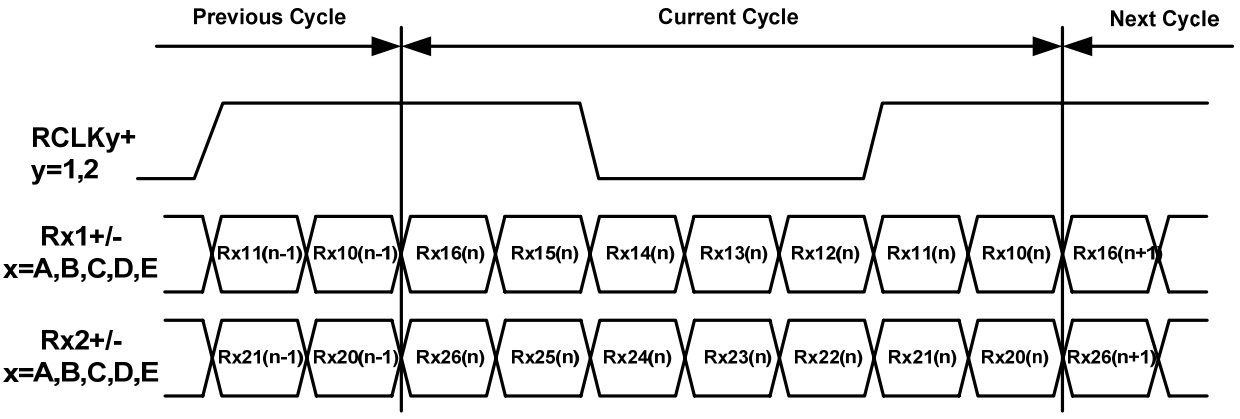


Figure 12.b. LVDS Inputs Mapped to TTL Data Outputs
MODE1 = L (Dual-in Mode) SEL = H



LVDS Input Data Mapping (Continued)

Table 5 : LVDS Input Data Mapping (Single-in/Single-out, MODE<1:0>=HH)

LVDS Input Data	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14	R12
RA11	R15	R13
RA12	R16	R14
RA13	R17	R15
RA14	R18	R16
RA15	R19	R17
RA16	G14	G12
RB10	G15	G13
RB11	G16	G14
RB12	G17	G15
RB13	G18	G16
RB14	G19	G17
RB15	B14	B12
RB16	B15	B13
RC10	B16	B14
RC11	B17	B15
RC12	B18	B16
RC13	B19	B17
RC14	HSYNC	HSYNC
RC15	VSYNC	VSYNC
RC16	DE	DE
RD10	R12	R18
RD11	R13	R19
RD12	G12	G18
RD13	G13	G19
RD14	B12	B18
RD15	B13	B19
RD16	CONT11	CONT11
RE10	R10	R10
RE11	R11	R11
RE12	G10	G10
RE13	G11	G11
RE14	B10	B10
RE15	B11	B11
RE16	CONT12	CONT12

LVDS Input Data Mapping (Continued)

Table 6 : LVDS Input Data Mapping (Single-in/Dual-out, MODE<1:0>=HL)

1'st Pixel Data			2'nd Pixel Data		
LVDS Input Data (1'st Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (2'nd Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10 (n)	R14	R12	RA10 (n+1)	R24	R22
RA11 (n)	R15	R13	RA11 (n+1)	R25	R23
RA12 (n)	R16	R14	RA12 (n+1)	R26	R24
RA13 (n)	R17	R15	RA13 (n+1)	R27	R25
RA14 (n)	R18	R16	RA14 (n+1)	R28	R26
RA15 (n)	R19	R17	RA15 (n+1)	R29	R27
RA16 (n)	G14	G12	RA16 (n+1)	G24	G22
RB10 (n)	G15	G13	RB10 (n+1)	G25	G23
RB11 (n)	G16	G14	RB11 (n+1)	G26	G24
RB12 (n)	G17	G15	RB12 (n+1)	G27	G25
RB13 (n)	G18	G16	RB13 (n+1)	G28	G26
RB14 (n)	G19	G17	RB14 (n+1)	G29	G27
RB15 (n)	B14	B12	RB15 (n+1)	B24	B22
RB16 (n)	B15	B13	RB16 (n+1)	B25	B23
RC10 (n)	B16	B14	RC10 (n+1)	B26	B24
RC11 (n)	B17	B15	RC11 (n+1)	B27	B25
RC12 (n)	B18	B16	RC12 (n+1)	B28	B26
RC13 (n)	B19	B17	RC13 (n+1)	B29	B27
RC14 (n)	HSYNC	HSYNC	RC14 (n+1)	HSYNC	HSYNC
RC15 (n)	VSYNC	VSYNC	RC15 (n+1)	VSYNC	VSYNC
RC16 (n)	DE	DE	RC16 (n+1)	DE	DE
RD10 (n)	R12	R18	RD10 (n+1)	R22	R28
RD11 (n)	R13	R19	RD11 (n+1)	R23	R29
RD12 (n)	G12	G18	RD12 (n+1)	G22	G28
RD13 (n)	G13	G19	RD13 (n+1)	G23	G29
RD14 (n)	B12	B18	RD14 (n+1)	B22	B28
RD15 (n)	B13	B19	RD15 (n+1)	B23	B29
RD16 (n)	CONT11	CONT11	RD16 (n+1)	CONT21	CONT21
RE10 (n)	R10	R10	RE10 (n+1)	R20	R20
RE11 (n)	R11	R11	RE11 (n+1)	R21	R21
RE12 (n)	G10	G10	RE12 (n+1)	G20	G20
RE13 (n)	G11	G11	RE13 (n+1)	G21	G21
RE14 (n)	B10	B10	RE14 (n+1)	B20	B20
RE15 (n)	B11	B11	RE15 (n+1)	B21	B21
RE16 (n)	CONT12	CONT12	RE16 (n+1)	CONT22	CONT22

LVDS Input Data Mapping (Continued)

Table 7 : LVDS Input Data Mapping

(Dual-in/Single-out, DDR On or Off, MODE<1:0>=LH, MODE2=H or L, MODE3 = H)

1'st Pixel Data			2'nd Pixel Data		
LVDS Input Data (1'st Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (2'nd Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14(n)	R12(n)	RA20	R14(n+1)	R12(n+1)
RA11	R15(n)	R13(n)	RA21	R15(n+1)	R13(n+1)
RA12	R16(n)	R14(n)	RA22	R16(n+1)	R14(n+1)
RA13	R17(n)	R15(n)	RA23	R17(n+1)	R15(n+1)
RA14	R18(n)	R16(n)	RA24	R18(n+1)	R16(n+1)
RA15	R19(n)	R17(n)	RA25	R19(n+1)	R17(n+1)
RA16	G14(n)	G12(n)	RA26	G14(n+1)	G12(n+1)
RB10	G15(n)	G13(n)	RB20	G15(n+1)	G13(n+1)
RB11	G16(n)	G14(n)	RB21	G16(n+1)	G14(n+1)
RB12	G17(n)	G15(n)	RB22	G17(n+1)	G15(n+1)
RB13	G18(n)	G16(n)	RB23	G18(n+1)	G16(n+1)
RB14	G19(n)	G17(n)	RB24	G19(n+1)	G17(n+1)
RB15	B14(n)	B12(n)	RB25	B14(n+1)	B12(n+1)
RB16	B15(n)	B13(n)	RB26	B15(n+1)	B13(n+1)
RC10	B16(n)	B14(n)	RC20	B16(n+1)	B14(n+1)
RC11	B17(n)	B15(n)	RC21	B17(n+1)	B15(n+1)
RC12	B18(n)	B16(n)	RC22	B18(n+1)	B16(n+1)
RC13	B19(n)	B17(n)	RC23	B19(n+1)	B17(n+1)
RC14	HSYNC(n)	HSYNC(n)	RC24	HSYNC(n+1)	HSYNC(n+1)
RC15	VSYNC(n)	VSYNC(n)	RC25	VSYNC(n+1)	VSYNC(n+1)
RC16	DE(n)	DE(n)	RC26	DE(n+1)	DE(n+1)
RD10	R12(n)	R18(n)	RD20	R12(n+1)	R18(n+1)
RD11	R13(n)	R19(n)	RD21	R13(n+1)	R19(n+1)
RD12	G12(n)	G18(n)	RD22	G12(n+1)	G18(n+1)
RD13	G13(n)	G19(n)	RD23	G13(n+1)	G19(n+1)
RD14	B12(n)	B18(n)	RD24	B12(n+1)	B18(n+1)
RD15	B13(n)	B19(n)	RD25	B13(n+1)	B19(n+1)
RD16	CONT11(n)	CONT11(n)	RD26	CONT11(n+1)	CONT11(n+1)
RE10	R10(n)	R10(n)	RE20	R10(n+1)	R10(n+1)
RE11	R11(n)	R11(n)	RE21	R11(n+1)	R11(n+1)
RE12	G10(n)	G10(n)	RE22	G10(n+1)	G10(n+1)
RE13	G11(n)	G11(n)	RE23	G11(n+1)	G11(n+1)
RE14	B10(n)	B10(n)	RE24	B10(n+1)	B10(n+1)
RE15	B11(n)	B11(n)	RE25	B11(n+1)	B11(n+1)
RE16	CONT12(n)	CONT12(n)	RE26	CONT12(n+1)	CONT12(n+1)

LVDS Input Data Mapping (Continued)

Table 8 : LVDS Input Data Mapping

(Dual-in/Single-out, DDR On or Off, MODE<1:0>=LH, MODE2=H or L, MODE3 = L)

1'st Pixel Data			2'nd Pixel Data		
LVDS Input Data (1'st Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (2'nd Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R24(n)	R22(n)	RA20	R24(n+1)	R22(n+1)
RA11	R25(n)	R23(n)	RA21	R25(n+1)	R23(n+1)
RA12	R26(n)	R24(n)	RA22	R26(n+1)	R24(n+1)
RA13	R27(n)	R25(n)	RA23	R27(n+1)	R25(n+1)
RA14	R28(n)	R26(n)	RA24	R28(n+1)	R26(n+1)
RA15	R29(n)	R27(n)	RA25	R29(n+1)	R27(n+1)
RA16	G24(n)	G22(n)	RA26	G24(n+1)	G22(n+1)
RB10	G25(n)	G23(n)	RB20	G25(n+1)	G23(n+1)
RB11	G26(n)	G24(n)	RB21	G26(n+1)	G24(n+1)
RB12	G27(n)	G25(n)	RB22	G27(n+1)	G25(n+1)
RB13	G28(n)	G26(n)	RB23	G28(n+1)	G26(n+1)
RB14	G29(n)	G27(n)	RB24	G29(n+1)	G27(n+1)
RB15	B24(n)	B22(n)	RB25	B24(n+1)	B22(n+1)
RB16	B25(n)	B23(n)	RB26	B25(n+1)	B23(n+1)
RC10	B26(n)	B24(n)	RC20	B26(n+1)	B24(n+1)
RC11	B27(n)	B25(n)	RC21	B27(n+1)	B25(n+1)
RC12	B28(n)	B26(n)	RC22	B28(n+1)	B26(n+1)
RC13	B29(n)	B27(n)	RC23	B29(n+1)	B27(n+1)
RC14	HSYNC(n)	HSYNC(n)	RC24	HSYNC(n+1)	HSYNC(n+1)
RC15	VSYNC(n)	VSYNC(n)	RC25	VSYNC(n+1)	VSYNC(n+1)
RC16	DE(n)	DE(n)	RC26	DE(n+1)	DE(n+1)
RD10	R22(n)	R28(n)	RD20	R22(n+1)	R28(n+1)
RD11	R23(n)	R29(n)	RD21	R23(n+1)	R29(n+1)
RD12	G22(n)	G28(n)	RD22	G22(n+1)	G28(n+1)
RD13	G23(n)	G29(n)	RD23	G23(n+1)	G29(n+1)
RD14	B22(n)	B28(n)	RD24	B22(n+1)	B28(n+1)
RD15	B23(n)	B29(n)	RD25	B23(n+1)	B29(n+1)
RD16	CONT21(n)	CONT21(n)	RD26	CONT21(n+1)	CONT21(n+1)
RE10	R20(n)	R20(n)	RE20	R20(n+1)	R20(n+1)
RE11	R21(n)	R21(n)	RE21	R21(n+1)	R21(n+1)
RE12	G20(n)	G20(n)	RE22	G20(n+1)	G20(n+1)
RE13	G21(n)	G21(n)	RE23	G21(n+1)	G21(n+1)
RE14	B20(n)	B20(n)	RE24	B20(n+1)	B20(n+1)
RE15	B21(n)	B21(n)	RE25	B21(n+1)	B21(n+1)
RE16	CONT22(n)	CONT22(n)	RE26	CONT22(n+1)	CONT22(n+1)

LVDS Input Data Mapping (Continued)

Table 9 : LVDS Input Data Mapping (Dual-in/Dual-out, MODE<1:0>=LL)

1'st Pixel Data			2'nd Pixel Data		
LVDS Input Data (1'st Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (2'nd Pixel)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14	R12	RA20	R24	R22
RA11	R15	R13	RA21	R25	R23
RA12	R16	R14	RA22	R26	R24
RA13	R17	R15	RA23	R27	R25
RA14	R18	R16	RA24	R28	R26
RA15	R19	R17	RA25	R29	R27
RA16	G14	G12	RA26	G24	G22
RB10	G15	G13	RB20	G25	G23
RB11	G16	G14	RB21	G26	G24
RB12	G17	G15	RB22	G27	G25
RB13	G18	G16	RB23	G28	G26
RB14	G19	G17	RB24	G29	G27
RB15	B14	B12	RB25	B24	B22
RB16	B15	B13	RB26	B25	B23
RC10	B16	B14	RC20	B26	B24
RC11	B17	B15	RC21	B27	B25
RC12	B18	B16	RC22	B28	B26
RC13	B19	B17	RC23	B29	B27
RC14	HSYNC	HSYNC	RC24	N/A	
RC15	VSYNC	VSYNC	RC25		
RC16	DE	DE	RC26		
RD10	R12	R18	RD20	R22	R28
RD11	R13	R19	RD21	R23	R29
RD12	G12	G18	RD22	G22	G28
RD13	G13	G19	RD23	G23	G29
RD14	B12	B18	RD24	B22	B28
RD15	B13	B19	RD25	B23	B29
RD16	CONT11	CONT11	RD26	CONT21	CONT21
RE10	R10	R10	RE20	R20	R20
RE11	R11	R11	RE21	R21	R21
RE12	G10	G10	RE22	G20	G20
RE13	G11	G11	RE23	G21	G21
RE14	B10	B10	RE24	B20	B20
RE15	B11	B11	RE25	B21	B21
RE16	CONT12	CONT12	RE26	CONT22	CONT22

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- The contents of this data sheet are subject to change without prior notice.

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