LVDS Product

DTC35LF36 (*Rev. 1.1*)

REVISED APR. 2009

+3.3V LVDS 30Bit Flat Panel Display (FPD) Receiver - 135MHz

General Description

The DTC35LF36 receivers convert the LVDS (Low Voltage Differential Signaling) data streams back into 35 bits of CMOS/TTL data with falling edge or rising edge clock for convenient interface with a variety of LCD panel controllers.

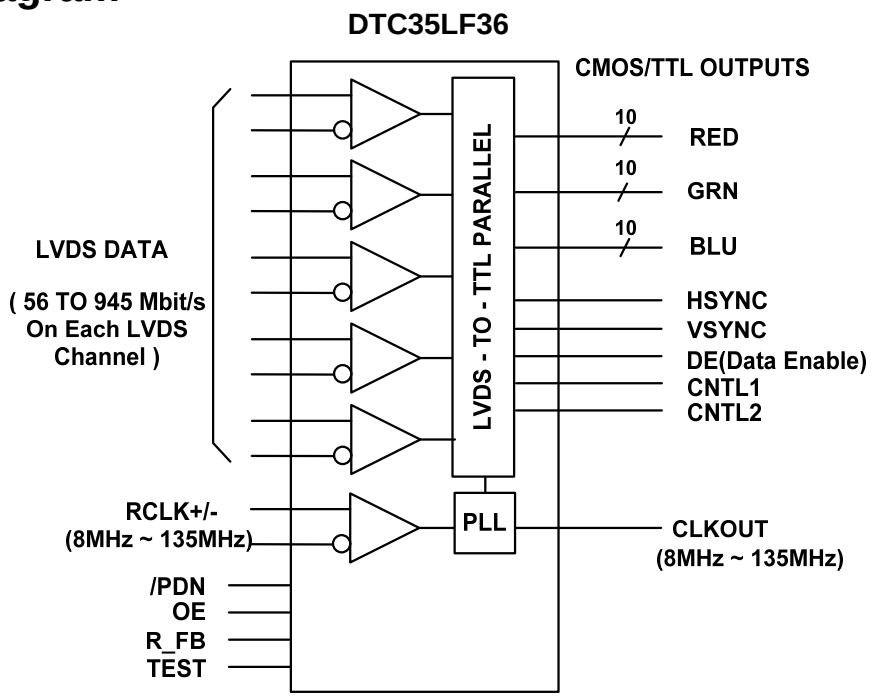
A phase-locked transmit clock is transmitted in parallel with the data streams over a sixth LVDS link. A transmitter (DTC35LM35) will inter-operate with a receiver (DTC35LF36) without any translation logic.

Using a 135 MHz clock, the data throughputs is 590.6 Mbytes/sec. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

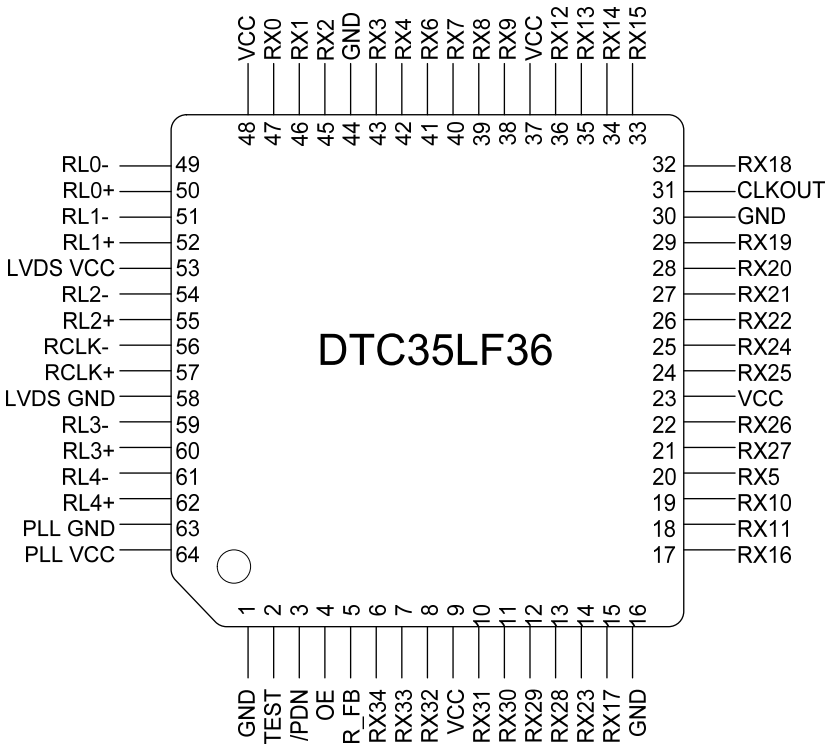
Features

- Wide frequency range : 8 to 135 MHz shift clock support
- Narrow bus (12 lines) reduces cable size
- Single 3.3V supply
- Power-Down Mode
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and SXGA
- Up to 590.6 Megabytes/sec bandwidth
- Up to 4.725 Gbps throughput
- 300mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 64-lead TQFP package
- Pin Compatible with Thine THC63LVD104
- Backward Compatible with DTC33LF86(18Bit)/DTC34LF86(24bit)

Block Diagram

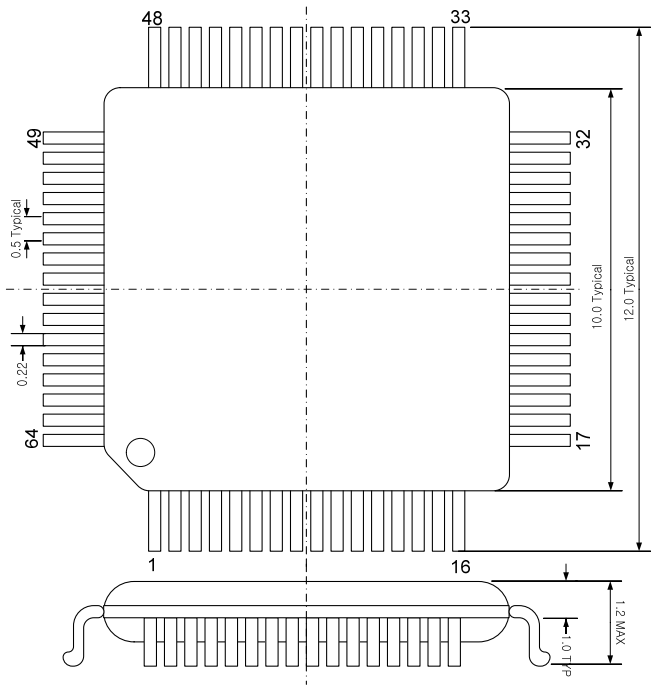


PIN OUT



PACKAGE

64 Pin TQFP Package, JEDEC [Unit : millimeters]



Electrical Characteristics

Vcc=3.0 ~ 3.6V @ Ta=-10 ~ +70°C

CMOS/TTL DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		Vcc	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -4mA(data) I_{OH} = -8mA(clock)	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 4mA(data) I_{OL} = 8mA(clock)			0.4	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ Vcc			±10	uA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			-50	mA

LVDS RECEIVER DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{OC} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{IN}	Input Current	V_{IN} = +2.4V/0V, Vcc = 3.6V			±10	uA

RECEIVER SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{RG}	Receiver Supply Current (16 Grayscale)	CL = 8pF, f = 90MHz, Vcc = 3.3V 16 Grayscale Pattern	77	83	mA
ICC_{RW}	Receiver Supply Current (Worst Case)	CL = 8pF, f = 90MHz, Vcc = 3.3V Worst Case Pattern	108	114	mA
ICC_{RP}	Receiver Supply Current (Power Down)	/PDN=0V	-	10	uA

Absolute Maximum Ratings (Note1)

Supply Voltage (Vcc) -0.3 to +4.0V
CMOS/TTL Input Voltage -0.3V to (Vcc + 0.3V)
CMOS/TTL Output Voltage -0.3V to (Vcc + 0.3V)
LVDS Driver Output Voltage -0.3V to (Vcc + 0.3V)
Output Short Circuit Duration Continuous
Junction Temperature +150°C
Storage Temperature Range –65°C to 150°C
Lead Temperature (Soldering, 4 sec.) +260°C
Maximum Power Dissipation @ 25°C 1.4W

(Note 1)

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation

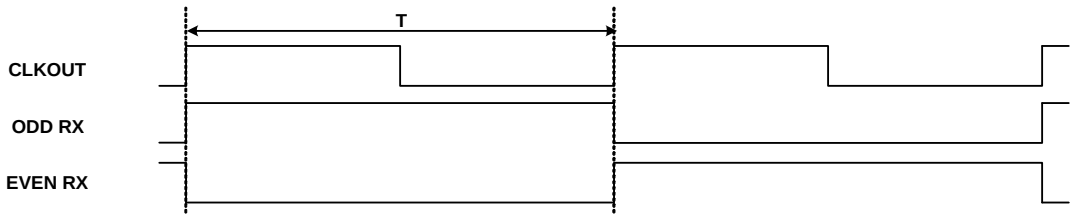
Receiver Switching Characteristics

Vcc=3.0 ~ 3.6V @ Ta=-10 ~ +70°C, T=1/f

Symbol	Parameter	Min	Typ	Max	Units
t_{RCP}	CLKOUT Period	7.4	T	125.0	nS
t_{RCH}	CLKOUT High Time		T/2		nS
t_{RCL}	CLKOUT Low Time		T/2		nS
t_{RCD}	RCLK+/- to CLKOUT Delay		7.0		nS
t_{RS}	TTL Data Setup to CLKOUT	4.0			nS
t_{RH}	TTL Data Hold from CLKOUT	0.4			nS
t_{TLH}	TTL Low to High Transition Time		2	3	nS
t_{THL}	TTL High to Low Transition Time		2	3	nS
t_{RDP5}	Receiver Input Data Position 0 (85MHz)	-0.25	0	0.25	nS
t_{RDP6}	Receiver Input Data Position 1 (85MHz)	T/7-0.25	T/7	T/7+0.25	nS
t_{RDP0}	Receiver Input Data Position 2 (85MHz)	2T/7-0.25	2T/7	2T/7+0.25	nS
t_{RDP1}	Receiver Input Data Position 3 (85MHz)	3T/7-0.25	3T/7	3T/7+0.25	nS
t_{RDP2}	Receiver Input Data Position 4 (85MHz)	4T/7-0.25	4T/7	4T/7+0.25	nS
t_{RDP3}	Receiver Input Data Position 5 (85MHz)	5T/7-0.25	5T/7	5T/7+0.25	nS
t_{RDP4}	Receiver Input Data Position 6 (85MHz)	6T/7-0.25	6T/7	6T/7+0.25	nS
t_{RPLLS}	Receiver Phase Lock Loop Set			10	mS

AC Timing Diagram

FIGURE 1. Test Pattern “Worst Case Pattern”



AC Timing Diagram(Continued)

FIGURE 2. Test Pattern "Grayscale Test Pattern"

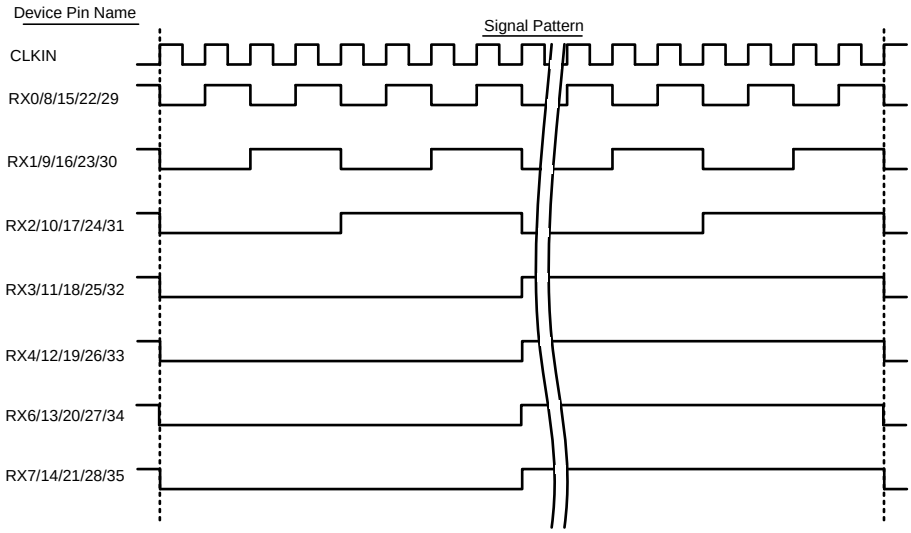


FIGURE 3. TTL Output

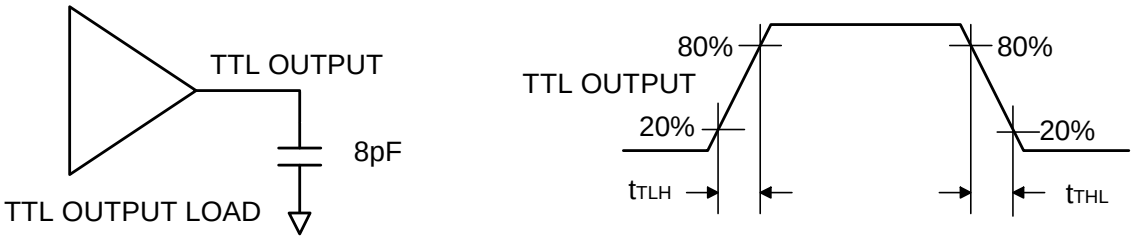
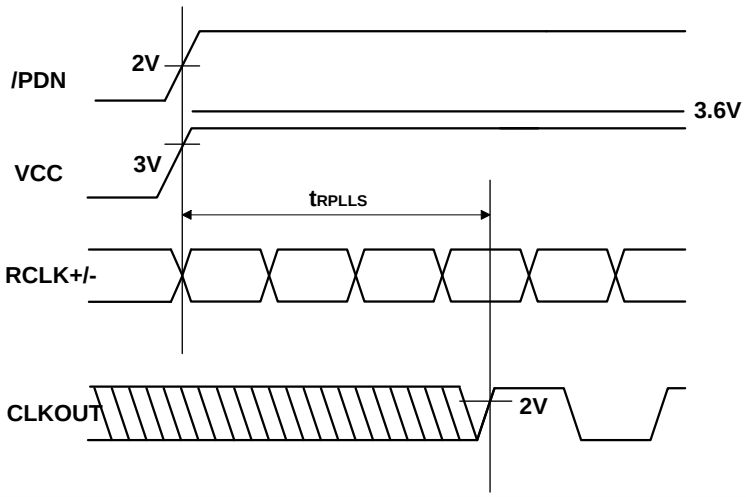
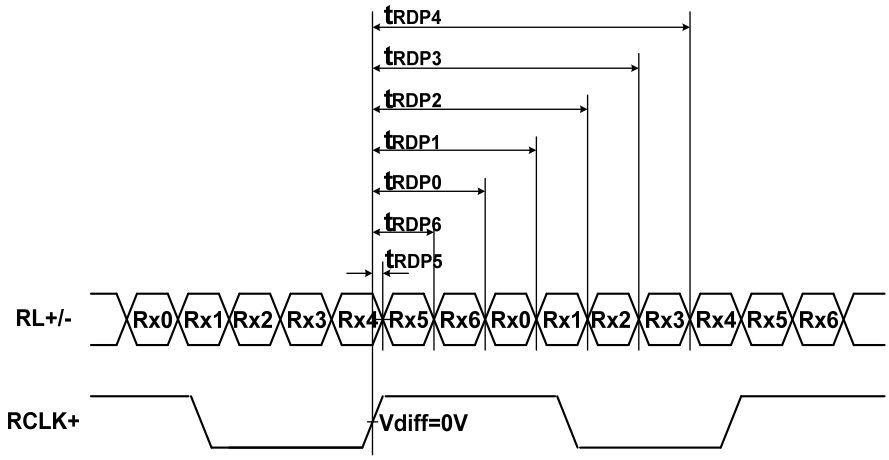


FIGURE 4. Phase Lock Loop Set Time



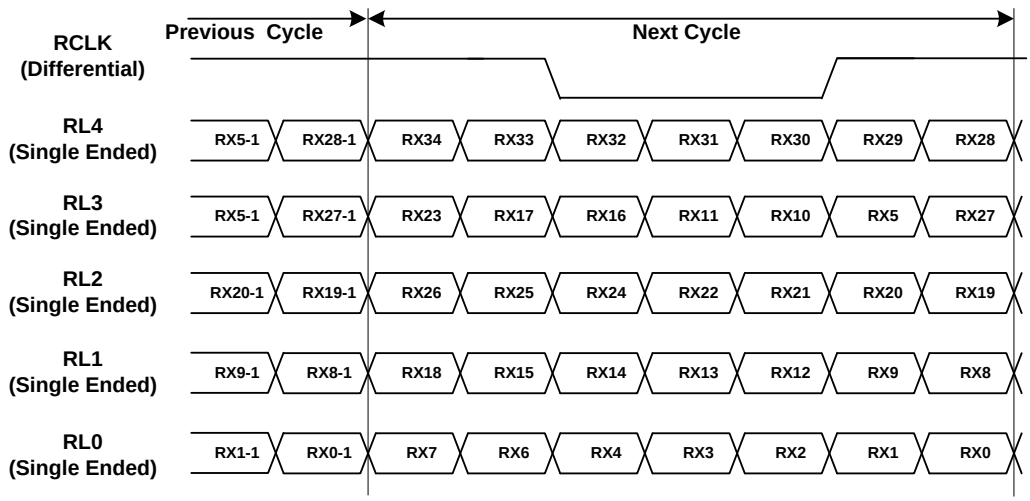
AC Timing Diagram(Continued)

FIGURE 5. Receiver Device Operation



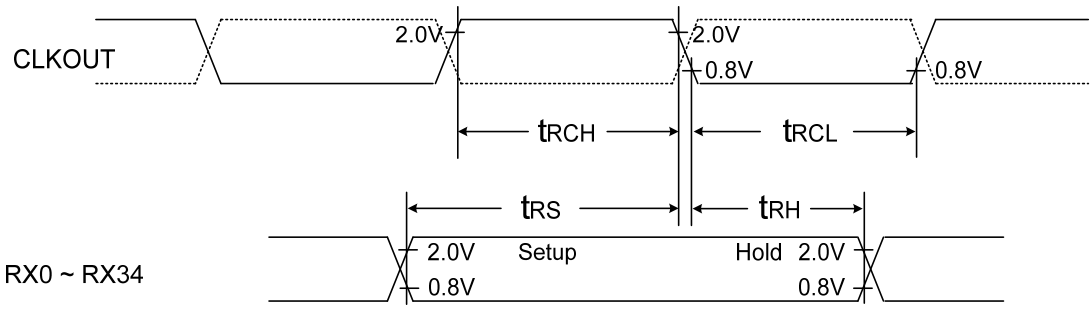
Note : **1) Vdiff = (RL+) - (RL-), ... (RCLK+) - (RCLK-)**

FIGURE 6. LVDS Inputs Mapped Parallel TTL Data Outputs



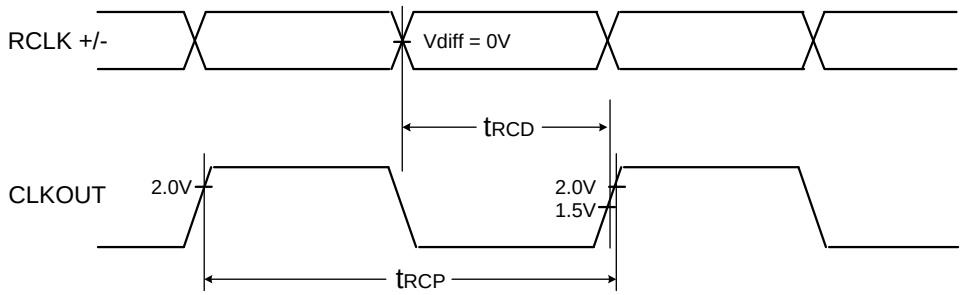
AC Timing Diagram (Continued)

FIGURE 7. Setup/Hold and High/Low Times



Note : **1) CLKOUT: for R_FB=GND, denoted as solid line(dotted line is for R_FB=VCC),**

FIGURE 8. RCLK to CLKOUT Delay



Note : **1) Vdiff = (RL+) - (RL-), ... (RCLK+) - (RCLK-)**

FIGURE 9. Package Pin Description

Pin Name	Pin #	Type	Description
RL0+,RL0-	49, 50	LVDS IN	LVDS differential data inputs.
RL1+, RL1-	51, 52	LVDS IN	
RL2+, RL2-	54, 55	LVDS IN	
RL3+, RL3-	59, 60	LVDS IN	
RL4+, RL4-	61, 32	LVDS IN	
RCLK+, RCLK-	56, 57	LVDS IN	LVDS differential clock inputs.
RX0 ~ RX6	47,46,45,43,42,20,41	OUT	TTL level data outputs. This includes : 10 Red, 10 Green, 10 Blue, and 5 control lines (HSYNC, VSYNC, DE, CNTL1, CNTL2)
RX7 ~ RX13	40,39,38,19,18,36,35	OUT	
RX14 ~ RX20	34,33,17,15,32,29,28	OUT	
RX21 ~ RX27	27,26,14,25,24,22,21	OUT	
RX28 ~ RX34	13,12,11,10,8,7,6	OUT	
CLKOUT	31	OUT	TTL level clock output. This falling edge acts as data strobe
/PDN	25	IN	TTL level input. H : Normal operation L : Power down (all outputs are low)
OE	4	IN	TTL level input. H : Output Enable (Normal operation) L : Output Disable (all outputs are Hi-Z)
R_FB	5	IN	TTL level input. Output Clock Triggering Edge Select. H : Rising Edge L : Falling Edge
SSCG_ON	2	IN	SSCG pin,"H" for SSCG ON, "L" for SSCG Off(Normal)
VCC	9,23,37,48	Power	Power supply pins for TTL outputs.
GND	1,16,30,44	Ground	Ground pins for TTL outputs.
LVDS VCC	53	Power	Power supply pin for LVDS inputs.
LVDS GND	58	Ground	Ground pins for LVDS inputs.
PLL VCC	64	Power	Power supply for PLL.
PLL GND	63	Ground	Ground pins for PLL.

/PDN	R_FB	OE	Data Outputs	Clock Outputs
0	0	0	Hi-Z	Hi-Z
0	0	1	All 0	Fixed Low
0	1	0	Hi-Z	Hi-Z
0	1	1	All 0	Fixed Low
1	0	0	Hi-Z	Hi-Z
1	0	1	Data Out	Negative Clock
1	1	0	Hi-Z	Hi-Z
1	1	1	Data Out	Positive Clock

IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.

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