LVDS Product

DTC14LM85M *(Rev.0.0)*

REVISED APR. 2012

+1.8V LVDS 24Bit Flat Panel Display (FPD) Transmitter - 180MHz

General Description

The DTC14LM85M transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A CLKIN signal is phase-locked and transmitted in parallel with the data streams over a fifth LVDS link. The frequency of TCLK+/- is the same as the input clock, CLKIN. 24 bits of graphic data, 3 bits of timing and 1 reserved data are transmitted at a rate of 1260Mbps per LVDS data channel at a transmit clock frequency of 180MHz. Using a 180MHz clock, the data throughput is 630Mbytes/sec. The RFB pin selects either rising or falling edge trigger of CLKIN. A Rising/Falling edge strobe transmitter will interoperate with a rising/falling edge strobe receiver without any translation logic. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces. The DTC14LM85M is available in 49pin FBGA.
The DTC14LM85M is quite suitable for mobile device such as like Tablet PC, MID owing to its low current consumption.

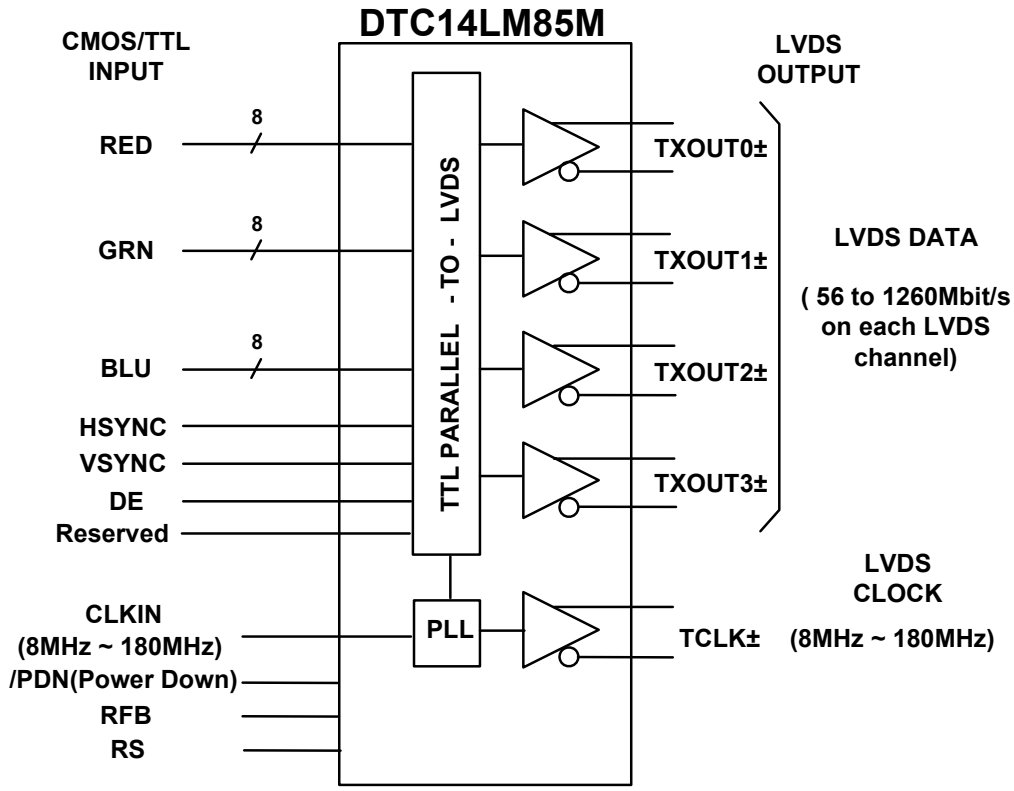
Features

- Wide frequency range: 8 to 180 MHz shift clock support
- Narrow bus (10 lines) reduces cable size and cost
- Power down mode
- Support QVGA - WUXGA and various resolutions.
- Supports spread spectrum clocking
- Supports data Inputs from 1.8V up to 3.3V
- Low current consumption for mobile application
- PLL requires no external components
- 5mm x 5mm/0.65mm pitch 49pin FBGA
- On chip input jitter filtering
- Up to 630 Mbytes/sec bandwidth
- Reduced swing LVDS support for low EMI (200mV or 350mV swing LVDS selectable)

Application

- Tablet PC, media tablet
- Mobile internet device
- Digital picture frame
- Smart phone
- Automobile
- Mobile TV
- Net book
- Navigation
- Various display devices

Block Diagram



Option Pin Information

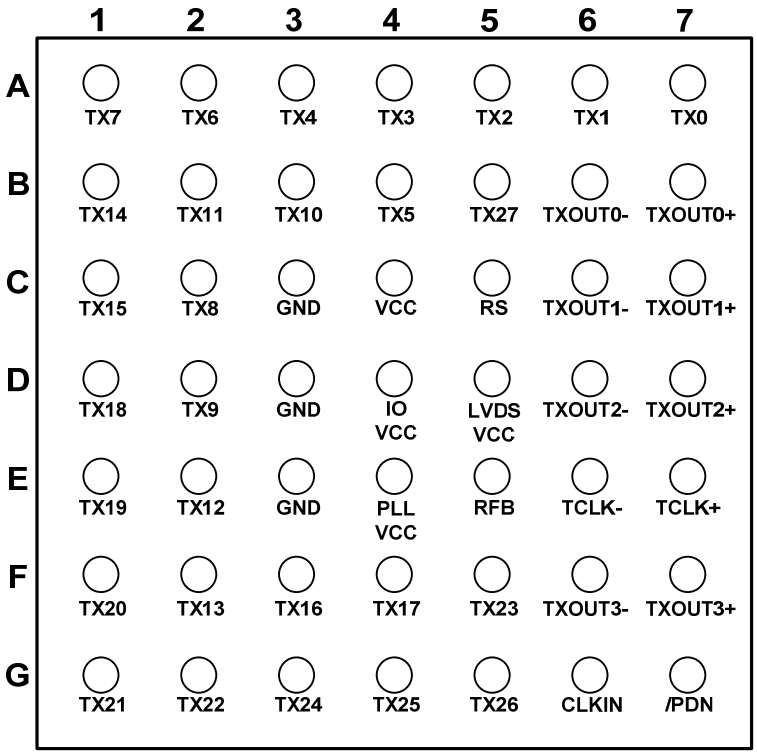
- The RS pin decides LVDS output swing level. (When the RS pin is 'IOVCC', LVDS output swing is 350mV)
- The RFB pin decides clock edge of input signals. (When the RFB pin is floating, falling edge is default.)
- The Reserved pin is not used for 24-bit color display. (If the RSVD is not used, it should be connected to GND)
- The /PDN pin controls power-down mode. (When the /PDN pin is 'GND', this chip operates in power down)

Ordering Information

Part number	Part marking	Package
DTC14LM85M	14LM85M in FBGA package	49-pin T&R

FBGA Pin Out

(Top View)



FBGA Pin List

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	TX7	A2	TX6	A3	TX4
A4	TX3	A5	TX2	A6	TX1
A7	TX0	B1	TX14	B2	TX11
B3	TX10	B4	TX5	B5	TX27
B6	TXOUT0-	B7	TXOUT0+	C1	TX15
C2	TX8	C3	GND	C4	VCC
C5	RS	C6	TXOUT1-	C7	TXOUT1+
D1	TX18	D2	TX9	D3	GND
D4	IOVCC	D5	LVDSVCC	D6	TXOUT2-
D7	TXOUT2+	E1	TX19	E2	TX12
E3	GND	E4	PLLVCC	E5	RFB
E6	TCLK-	E7	TCLK+	F1	TX20
F2	TX13	F3	TX16	F4	TX17
F5	TX23	F6	TXOUT3-	F7	TXOUT3+
G1	TX21	G2	TX22	G3	TX24
G4	TX25	G5	TX26	G6	CLKIN
G7	/PDN	-	-	-	-

Electrical Characteristics

Supply Voltage DC Specification

Symbol	Parameter	Min	Typ	Max	Units
VCC	TTL input supply voltage	1.62	1.8	1.98	V
LVDSVCC	LVDS output supply voltage	1.62	1.8	1.98	V
PLLVCC	PLL supply voltage	1.62	1.8	1.98	V
IOVCC	IO supply voltage	1.62	1.8/2.5/3.3	3.6	V

CMOS/TTL DC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage	IOVCC=1.62~1.98V	IOVCC/2+0.2			V
		IOVCC=2.3~2.7V	IOVCC/2+0.3			
		IOVCC=3.0~3.6V	IOVCC/2+0.4			
V_{IL}	Low level input voltage	IOVCC=1.62~1.98V			IOVCC/2-0.3	V
		IOVCC=2.3~2.7V			IOVCC/2-0.4	
		IOVCC=3.0~3.6V			IOVCC/2-0.5	
I_{IN}	Input current	$0V \le V_{IN} \le$ IOVCC	-10		+10	uA

LVDS Transmitter DC Specification

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential output voltage	RL=100Ω	Normal Swing RS=H	250	350	450	mV
			Reduced Swing RS=L	100	200	300	mV
ΔV_{OD}	Change in V_{OD} between Complementary output states	RL=100Ω				35	mV
V_{OC}	Common mode voltage			1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between Complementary output states					35	mV
I_{OZ}	Output tri-state current	/PDN=0V, Vout=0V to Vcc		-20		+20	uA

Transmitter Supply Current

Symbol	Parameter	Conditions			Typ	Max	Units
ICC_{TG}	Transmitter supply current (16 Grayscale) [FIGURE2]	RL=100Ω CL = 5pF	Normal swing RS=H	f=85MHz	24		mA
				f=150MHz	41		
			Reduced swing RS=L	f=85MHz	19		
				f=150MHz	36		
ICC_{TW}	Transmitter supply current (Worst case) [FIGURE1]	RL=100Ω CL = 5pF	Normal swing RS=H	f=85MHz	27		
				f=150MHz	44		
			Reduced swing RS=L	f=85MHz	22		
				f=150MHz	39		
ICC_{TP}	Transmitter supply current (Power down)	/PDN=0V				50	uA

* All Typ. values are Vcc = 1.8V, Ta = 25°C

* All Max. values are Vcc = 1.98V, Ta = 85°C

Recommended Operating Conditions

Parameter		Min	Typ	Max	Units
Supply voltage (IOVCC)		1.62	1.8/2.5/3.3	3.6	V
Supply voltage (VCC,PLLVCC,LVDSVCC)		1.62	1.8	1.98	V
Operating ambient temperature (Ta)		-40		85	°C
Clock frequency	Input	8		180	MHz
	LVDS output	8		180	MHz

Absolute Maximum Ratings (Note1)

Supply voltage(IOVCC)	-0.3 to +4V
Supply voltage(VCC,PLLVCC,LVDSVCC)	-0.3 to +2.1V
CMOS/TTL input voltage	-0.3V to (IOVCC + 0.3V)
LVDS driver output voltage	-0.3V to (Vcc + 0.3V)
Junction temperature	+125 °C
Storage temperature range	-55 °C to 125 °C
Reflow peak temperature (Soldering, 10 sec.)	+260 °C
Maximum power dissipation @25°C	1.4W

(Note 1)

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

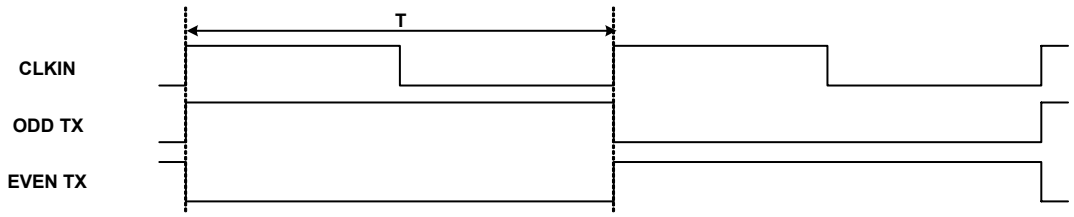
Transmitter Switching Characteristics

VCC=LVDSVCC=PLLVCC= 1.62~1.98V, IOVCC=1.62~3.6V, Ta=-40 ~ +85°C, T=1/f

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLKIN transition time			1.25	ns
t_{TCP}	CLKIN period	5.5	T	125	ns
t_{TCH}	CLKIN high time	0.4T	0.5T	0.6T	ns
t_{TCL}	CLKIN low time	0.4T	0.5T	0.6T	ns
t_{TCD}	CLKIN to TCLK+/- delay		2T/7 + 2.3		ns
t_{TS}	TTL data setup to CLKIN	0.8			ns
t_{TH}	TTL data hold from CLKIN	0.8			ns
t_{LVT}	LVDS transition time		0.15	0.4	ns
t_{TDP1}	Transmitter output data position 0 (180MHz)	-0.1	0	0.1	ns
t_{TDP0}	Transmitter output data position 1 (180MHz)	T/7-0.1	T/7	T/7+0.1	ns
t_{TDP6}	Transmitter output data position 2 (180MHz)	2T/7-0.1	2T/7	2T/7+0.1	ns
t_{TDP5}	Transmitter output data position 3 (180MHz)	3T/7-0.1	3T/7	3T/7+0.1	ns
t_{TDP4}	Transmitter output data position 4 (180MHz)	4T/7-0.1	4T/7	4T/7+0.1	ns
t_{TDP3}	Transmitter output data position 5 (180MHz)	5T/7-0.1	5T/7	5T/7+0.1	ns
t_{TDP2}	Transmitter output data position 6 (180MHz)	6T/7-0.1	6T/7	6T/7+0.1	ns
t_{TPLLS}	Transmitter phase lock loop set	-	-	10	ms

AC Timing Diagrams

FIGURE 1. Test Pattern “Worst Case Pattern”



AC Timing Diagrams (Continued)

FIGURE 2. Test Pattern "16 Grayscale Test Pattern"

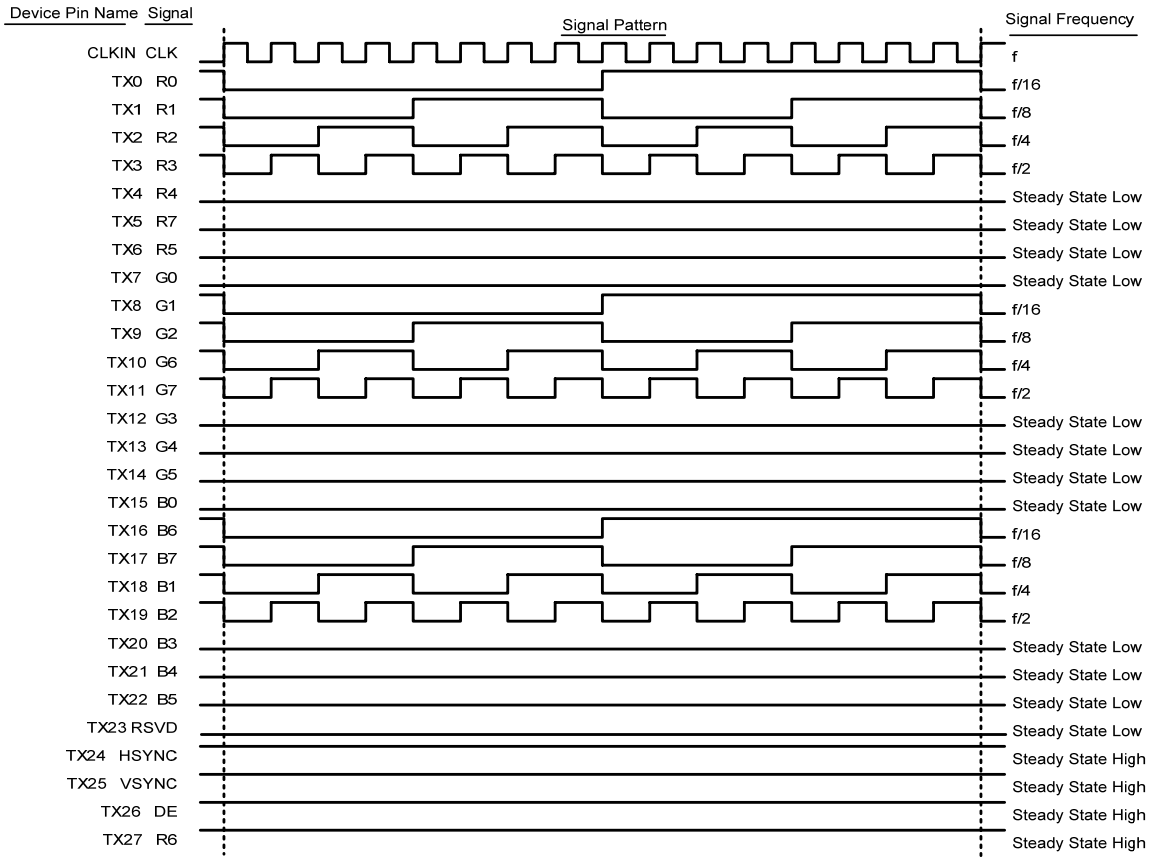


FIGURE 3. TTL Input

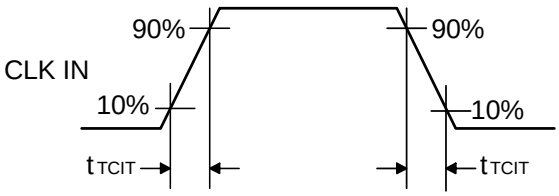
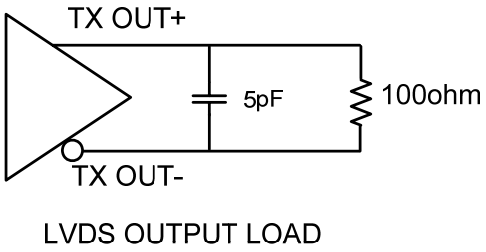
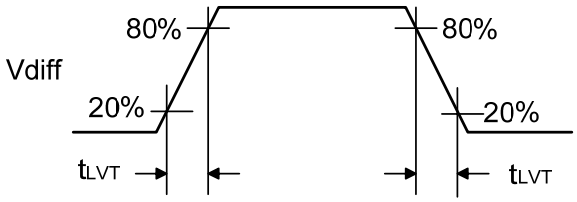


FIGURE 4. LVDS Output

Vdiff= (TXOUT+) – (TXOUT–)



LVDS OUTPUT LOAD



AC Timing Diagrams (Continued)

FIGURE 5. Phase Lock Loop Set Time

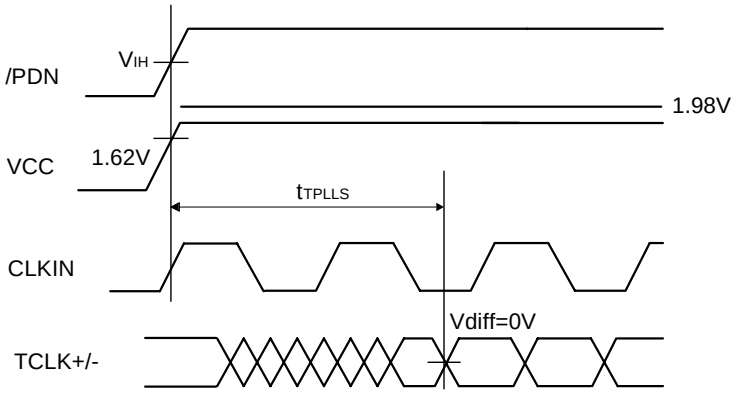
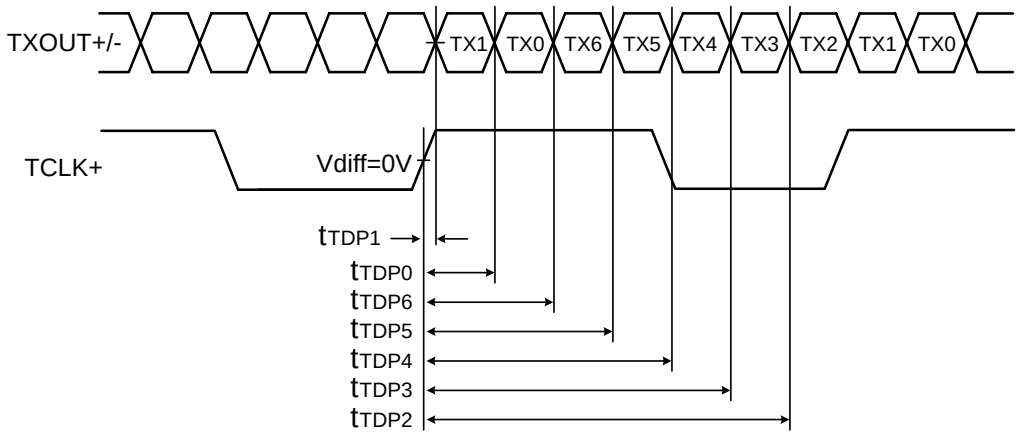


FIGURE 6. Transmitter Device Operation



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) – (TCLK-)**

FIGURE 7. Parallel TTL Data Inputs Mapped to LVDS Outputs – DTC14LM85M

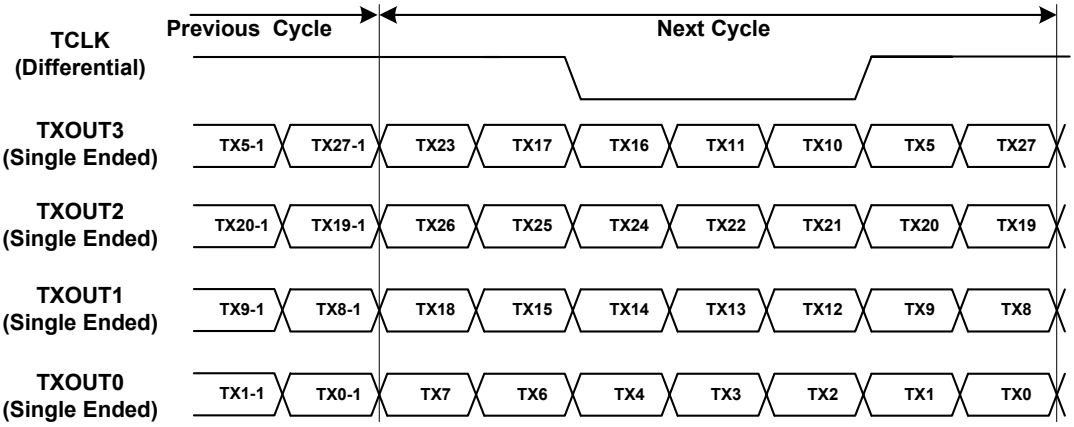
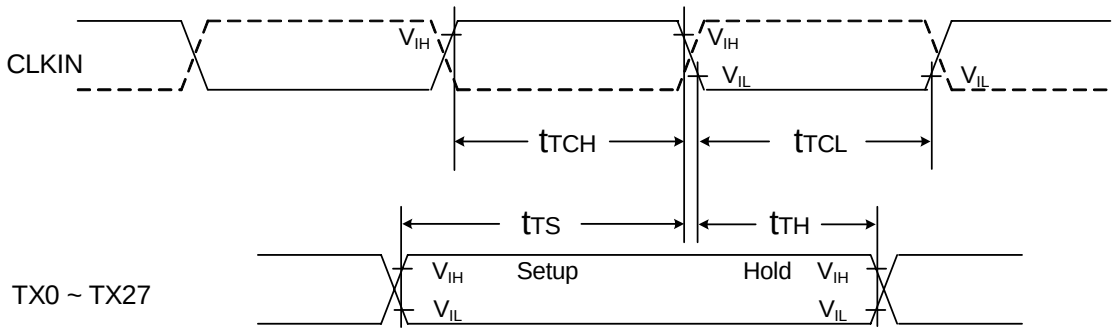


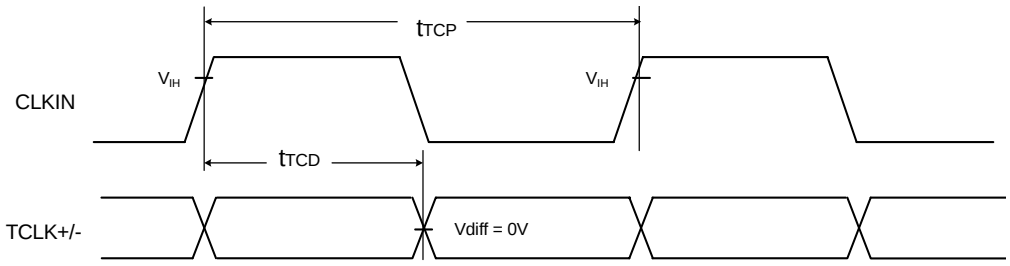
FIGURE 8. Setup/Hold and High/Low Times



Note : **1) CLKIN : for DTC14LM85M(RFB=GND), denoted as solid line**

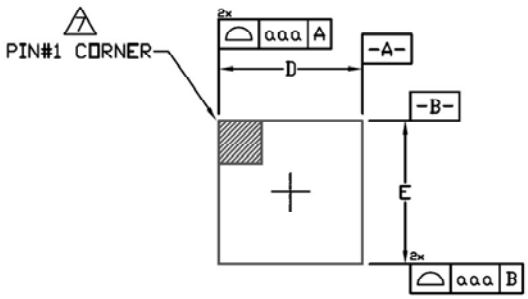
for DTC14LM85M(RFB=IOVCC), denoted as dotted line

FIGURE 9. CLKIN to CLKOUT Delay

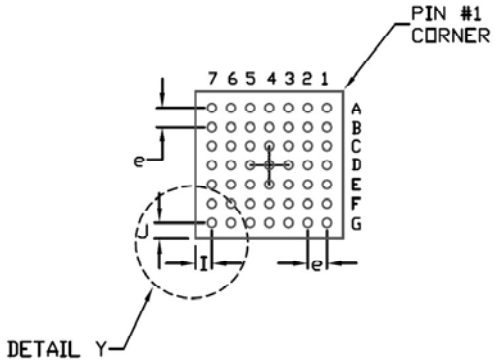


Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) - (TCLK-)**

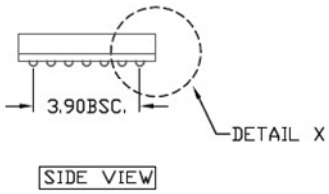
FBGA PACKAGE



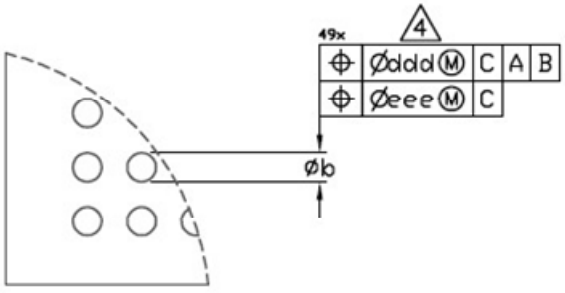
TOP VIEW



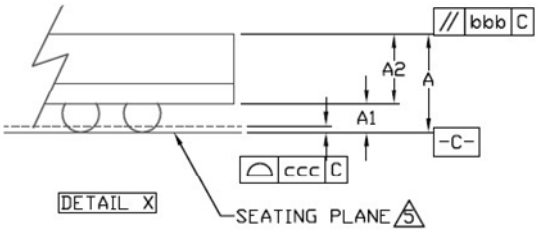
BOTTOM VIEW



SIDE VIEW



DETAIL Y



SYMBOL	MIN.	NOM.	MAX.
A	–	–	1.30
A1	0.17	0.22	–
A2	–	0.96	–
D	4.90	5.00	5.10
E	4.90	5.00	5.10
I		0.55 REF.	
J		0.55 REF.	
M		7X7<FULL>	
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.15
eee			0.05
b	0.25	0.30	0.35
e		0.65 BSC.	
c		0.26 REF.	

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DEMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C- .
5. PRIMARY DATUM -C- AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
7. A1 CORNER MUST BE IDENTIFIED BY LASER MARK.
8. PACKAGE DIMENSIONS CONFORM TO JEDEC REGISTRATION MO–225.

APPLICATION INFORMATION

This application note's purpose is not to specify a strict circuit implementation of a display system using the DTC FPD Interface chipset family, but to provide some guidelines for successful implementation of it.

System Designing Considerations

PCB Layout Considerations

Lines of a LVDS differential signal pair should always be adjacent to eliminate noise interference from other signals and effectively cancel the noise on the differential signals.

The physical length of PCB trace for a given LVDS differential signal pair should be matched as much as possible.

The physical length of PCB trace for each LVDS differential signal pairs should be keep as short as possible; otherwise the differential impedance of PCB must be controlled to be near 100 Ohm.

The physical length of PCB trace of CMOS/TTL signals should be keep as short and close to the same as possible. The PCB trace of CMOS/TTL signals should be isolated from LVDS differential signal pairs, placing them at least "3s" or "2w" away (see Figure 10).

To limit the impedance discontinuities causing signal reflection and crosstalk, the 90° angle on PCB trace must be not used (see Figure 11) and the number of via should be reduced.

If any impedance discontinuities occur on one signal line, it must be mirrored in the other line of the differential pair.

These considerations reduce the signal reflection and crosstalk, and make it helpful to obtain full benefit of the noise and EMI reduction from LVDS.

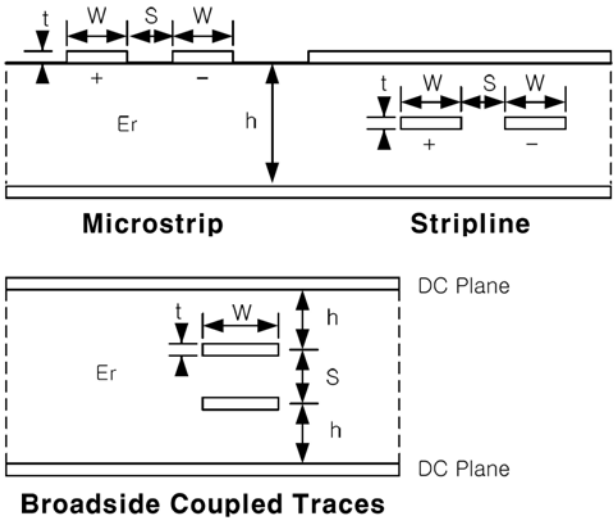


Figure10. PCB Construct Cross-section

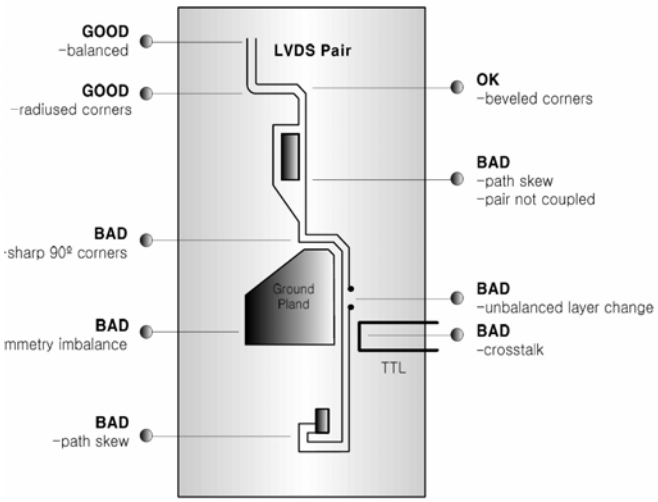


Figure11. PCB Layout Example

Termination

Because of using current mode output driver in LVDS, a termination resistor is required across the receiver's differential input pair per channel and its typical value is 100 ohms (see Figure 12).

These termination resistors should be placed as close as possible to the receiver's input pins to shorten stubs and effectively terminate the differential lines.

For the type of resistor, surface mount resistors are recommended rather than leaded resistors to avoid additional parasitic inductance.

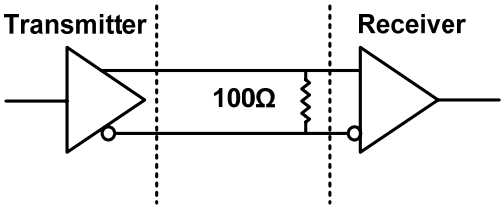


Figure12. LVDS Differential Termination

Power & Ground

Power supply system performance can be greatly improved by bypassing capacitors that reduce the impact of switching noise and its feedback or interference between different blocks of the circuits.

In general, each VCC pins are required to have separate bypassing sufficient to ensure less than 100 mV peak-to-peak noises on the supply pins.

Power Up Sequencing

A specific power up sequence is not required in the DTC FPD Interface chipset family. But the best practice is: power up all VCC together, apply clocks, and then assert /PDN power-down pins high to enable the transmitter and/or receiver.

The /PDN pin is internally pulled down to ground that the device is disabled if this pin is left open circuited.

When powering down the device, the transmitter outputs remain in tri-state and the receiver outputs are low.

When the device are actively driven, the /PDN pin should be pulled up to VCC by no more than a 10 kOhms resistor.

Falling edge or Rising edge Selection

The DTC FPD receivers are available with either a falling edge data strobe or a rising edge data strobe, which is selectable according to the LCD panel timing controller requirements. The strobe edge only affects the TTL inputs of the transmitter or outputs of the receiver, while the LVDS interface is not affected.

Bit Mapping of FPD Interface Data

The transmitter's data input from the graphic controller consist of 18 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, and an enable bit for 18-bit device, or consist of 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit , and a spare bit for 24-bit device. Only three LVDS data channels are required for and 18-bit FPD interface application.

The most significant bits (MSB) for an 18-bit application must be mapped exactly the same as the most significant bits in the 24-bit application, and additional least significant in the 24-bit application are mapped the 4th LVDS data channel.

The output of the receiver to LCD panel controller has same bit mapping as the input to the transmitter.

The detailed bit mapping information between the RGB data of graphic information and the CMOS/TTL data pins of the transmitter/receiver is listed in Table 1, and that between the data arrangement of LVDS channels and the CMOS/TTL data pins of the transmitter/receiver is also described in Figure 13 and Figure 14.

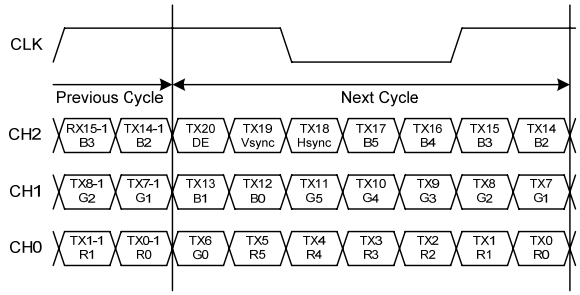


Figure13. Bit Mapping between LVDS and CMOS/TTL signals for 18-bit Color Display

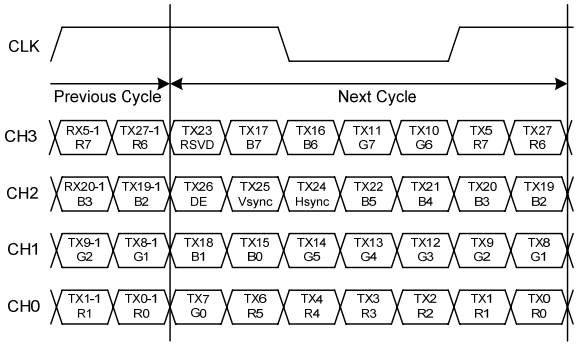


Figure14. Bit Mapping between LVDS and CMOS/TTL signals for 24-bit Color Display

24bit FPD Interface Application

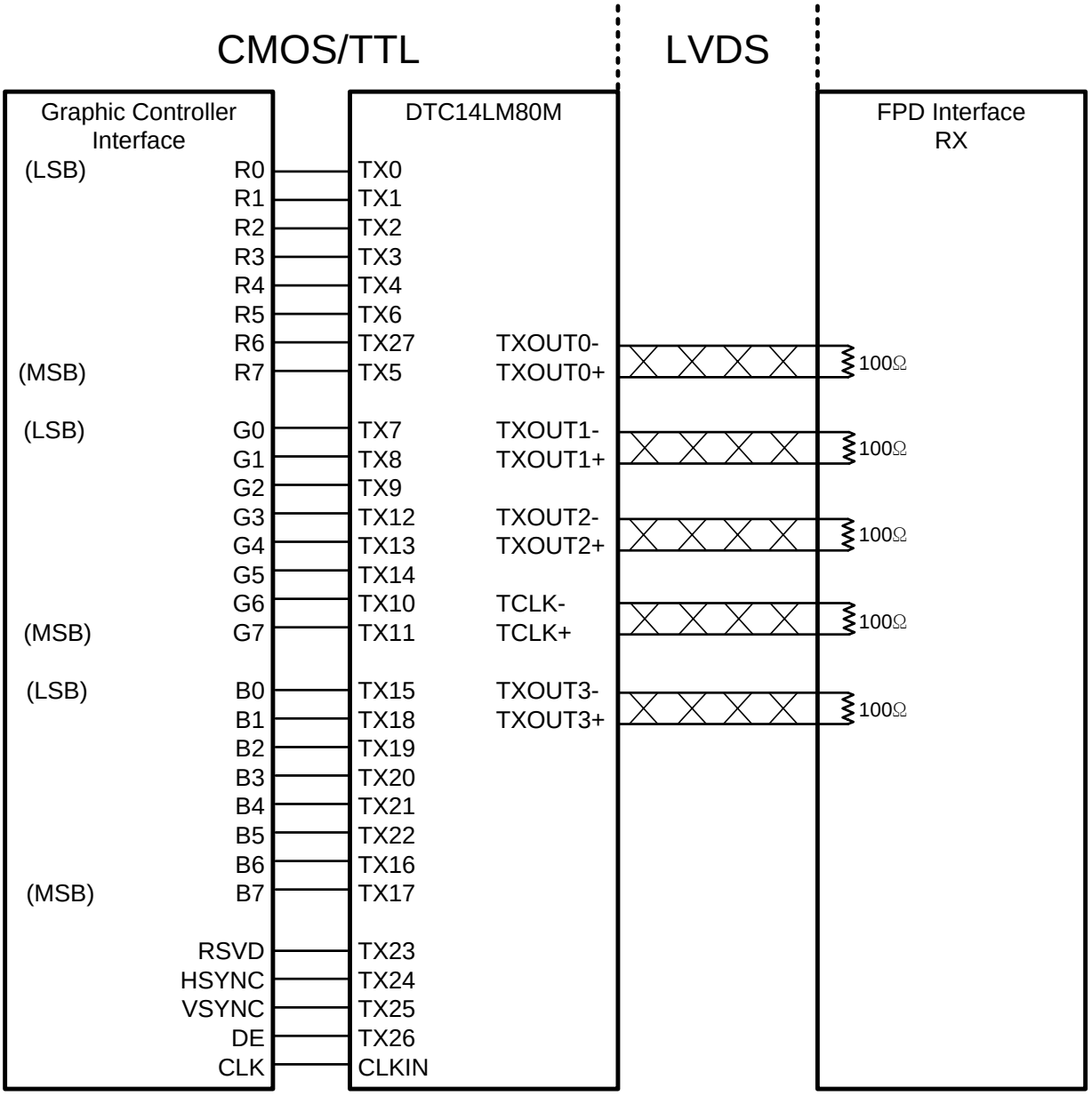


Figure15. 24bit FPD interface Application

18bit FPD Interface Application

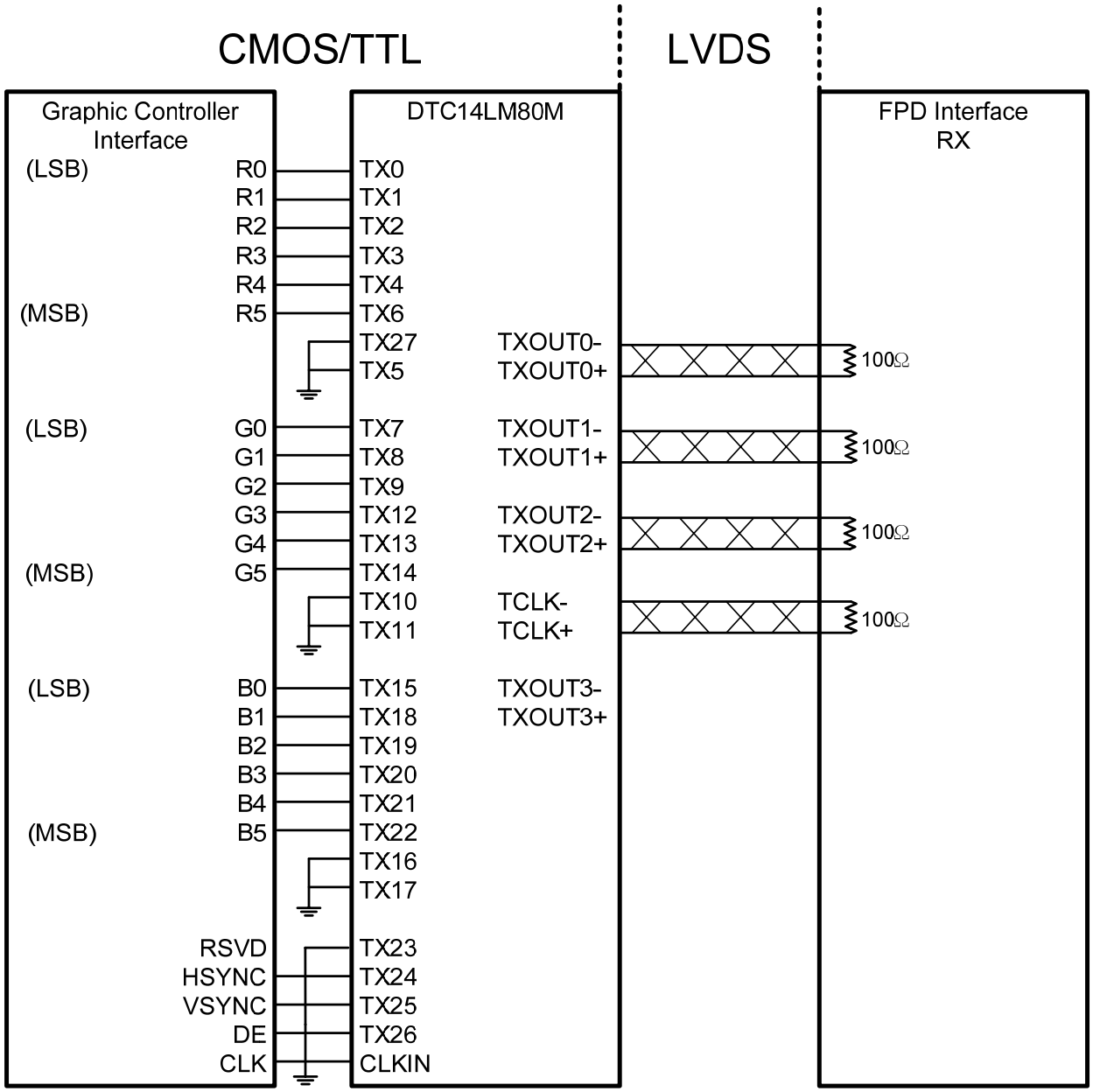


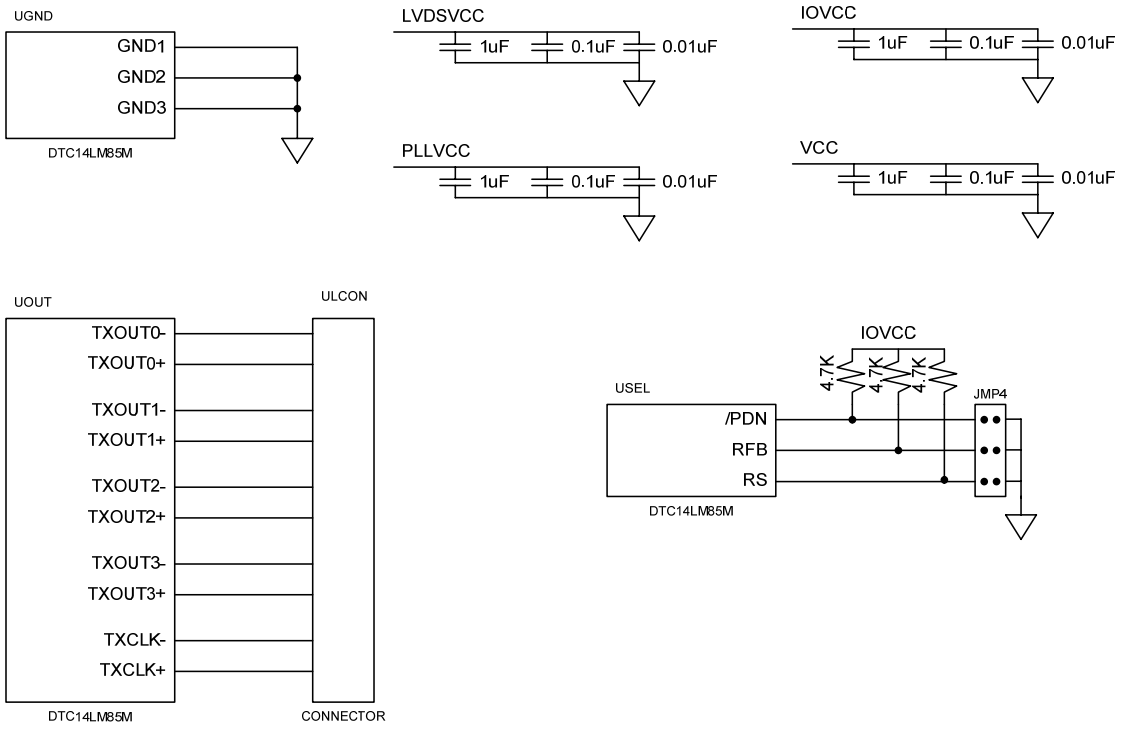
Figure16. 18bit FPD interface Application

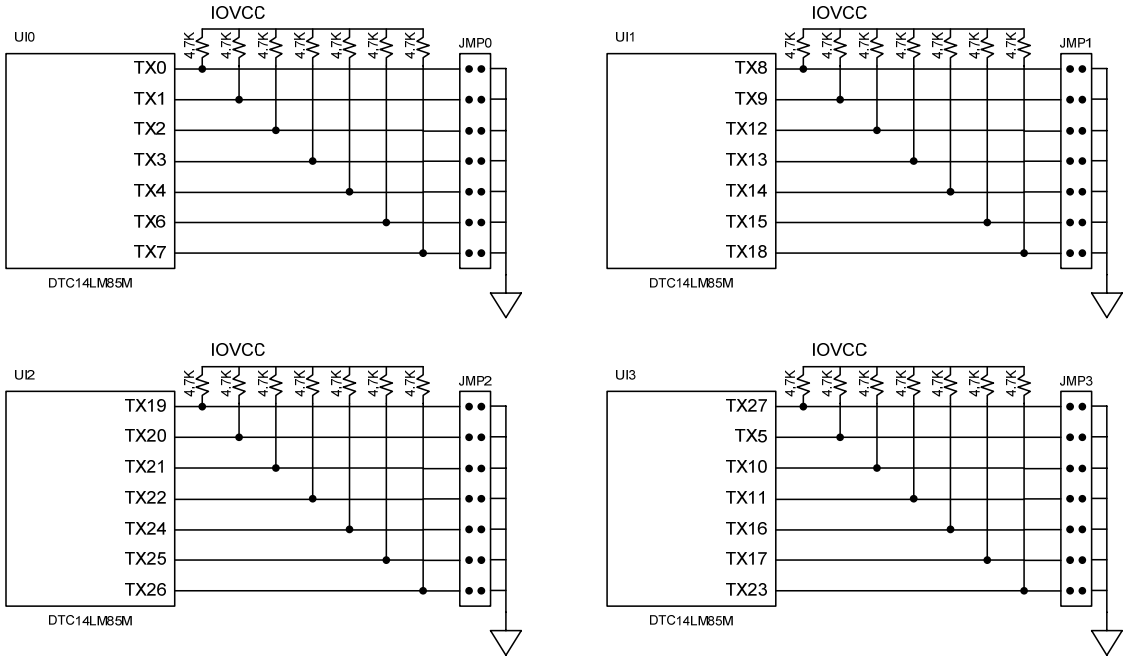
Bit Mapping for 18-bit and 24-bit Color Display

VGA-TFT Data Signal			Transmitter Input Data Pin		Receiver Output Data Pin		TFT Panel Data Signal	
	24-bit	18-bit	24-bit Tx (14LM80)	18-bit Tx	24-bit Rx	18-bit Rx	18-bit	24-bit
LSB	R0		TX0		RX0			R0
	R1		TX1		RX1			R1
	R2	R0	TX2	TX0	RX2	RX0	R0	R2
	R3	R1	TX3	TX1	RX3	RX1	R1	R3
	R4	R2	TX4	TX2	RX4	RX2	R2	R4
	R5	R3	TX6	TX3	RX6	RX3	R3	R5
	R6	R4	TX27	TX4	RX27	RX4	R4	R6
MSB	R7	R5	TX5	TX5	RX5	RX5	R5	R7
LSB	G0		TX7		RX7			G0
	G1		TX8		RX8			G1
	G2	G0	TX9	TX6	RX9	RX6	G0	G2
	G3	G1	TX12	TX7	RX12	RX7	G1	G3
	G4	G2	TX13	TX8	RX13	RX8	G2	G4
	G5	G3	TX14	TX9	RX14	RX9	G3	G5
	G6	G4	TX10	TX10	RX10	RX10	G4	G6
MSB	G7	G5	TX11	TX11	RX11	RX11	G5	G7
LSB	B0		TX15		RX15			B0
	B1		TX18		RX18			B1
	B2	B0	TX19	TX12	RX19	RX12	B0	B2
	B3	B1	TX20	TX13	RX20	RX13	B1	B3
	B4	B2	TX21	TX14	RX21	RX14	B2	B4
	B5	B3	TX22	TX15	RX22	RX15	B3	B5
	B6	B4	TX16	TX16	RX16	RX16	B4	B6
MSB	B7	B5	TX17	TX17	RX17	RX17	B5	B7
	RSVD		TX23		RX23			RSVD
	Hsync	Hsync	TX24	TX18	RX24	RX18	Hsync	Hsync
	Vsync	Vsync	TX25	TX19	RX25	RX19	Vsync	Vsync
	DE	DE	TX26	TX20	RX26	RX20	DE	DE

Table1. Bit Mapping for 18bit and 24bit Color Display.

Typical Application Schematic





Package Pin Description

Pin Name	Pin #	Type	Description
TXOUT0-, TXOUT0+	B6,B7	LVDS OUT	LVDS differential data outputs.
TXOUT1-, TXOUT1+	C6,C7	LVDS OUT	
TXOUT2-, TXOUT2+	D6,D7	LVDS OUT	
TXOUT3-, TXOUT3+	F6,F7	LVDS OUT	
TCLK-, TCLK+	E6,E7	LVDS OUT	LVDS differential clock outputs.
TX0 ~ TX6	A7,A6,A5,A4,A3,B4,A2	IN	Data inputs. This includes : 8 Red, 8 Green, 8 Blue, and 3 control lines (HSYNC, VSYNC, DE) and 1 Reserved
TX7 ~ TX13	A1,C2,D2,B3,B2,E2,F2	IN	
TX14 ~ TX20	B1,C1,F3,F4,D1,E1,F1	IN	
TX21 ~ TX27	G1,G2,F5,G3,G4,G5,B5	IN	
CLKIN	G6	IN	Clock input. This falling edge acts as data strobe
/PDN	G7	IN	Power down control /PDN=IOVCC : Normal operation /PDN=GND : Power down (all output are low)
RFB	E5	IN	Programmable strobe select. RFB=IOVCC :Rising edge, RFB=GND:Falling edge
RS	C5	IN	LVDS swing mode select RS=IOVCC :350mV, RS=GND:200mV
VCC	C4	Power	Power supply pins for digital.
GND	C3,D3,E3	Ground	Ground pins for digital.
LVDSVCC	D5	Power	Power supply pin for LVDS outputs.
PLLVCC	E4	Power	Power supply pin for PLL.
IOVCC	D4	Power	Power pin for IO.

Table2. Package Pin Description

IMPORTANT NOTICE:

- The contents of this data sheet are subject to change without prior notice.

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