LVDS Product

DTC34LM85AM(R) *(Rev. 0.3)*

REVISED APR. 2011

+3.3V LVDS 24Bit Flat Panel Display (FPD) Transmitter - 135MHz

General Description

The DTC34LM85AM(R) transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A CLKIN signal is phase-locked and transmitted in parallel with the data streams over a fifth LVDS link. The frequency of TCLK+/- is the same as the input clock, CLKIN. 24 bits of graphic data and 3 bits of timing and 1 control data are transmitted at a rate of 945 Mbps per LVDS data channel at a transmit clock frequency of 135MHz. Using a 135 MHz clock, the data throughput is 472.5 Mbytes/sec. The R_FB pin selects either rising or falling edge trigger of CLKIN. A Rising/Falling edge strobe transmitter will interoperate with a Rising/Falling edge strobe receiver (DTC34LF/R86L) without any translation logic. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces. The DTC34LM85AM(R) is available in both FBGA and TSSOP package.

The DTC34LM85AM(R) is quite suitable for mobile device such as like Tablet PC, MID owing to its low current consumption

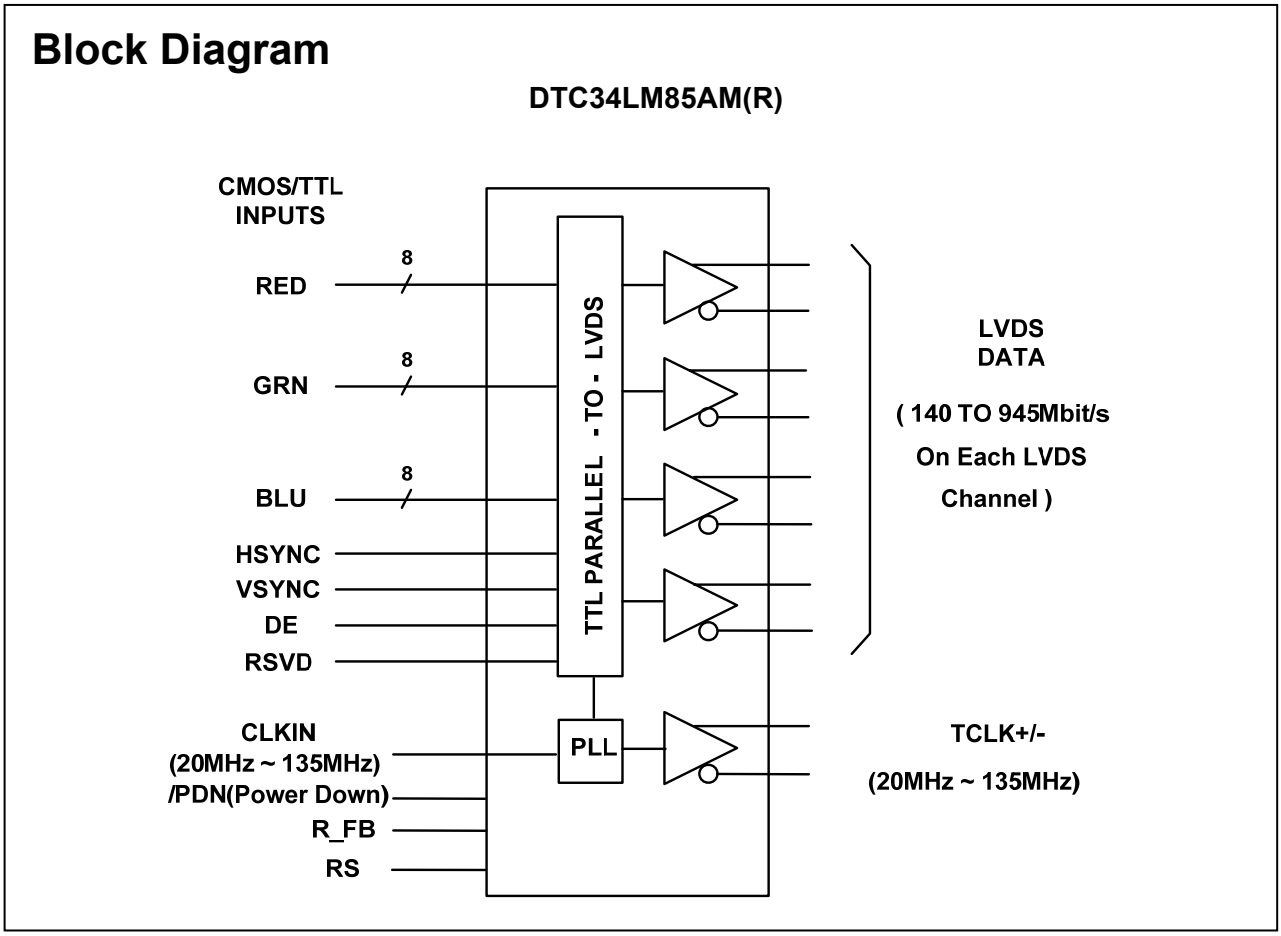
Features

- Wide frequency range: 20 to 135 MHz shift clock support
- Narrow bus (10 lines) reduces cable size and cost
- Power-Down Mode
- Support VGA, WVGA, SVGA, XGA, WXGA, SXGA, WSXGA, UXGA, HD and various resolutions.
- Supports Spread Spectrum Clocking
- Supports Data Inputs from 1.8V up to 3.3V
- On Chip Input Jitter Filtering
- Up to 472.5 Megabytes/sec bandwidth
- Reduced Swing LVDS Support for low EMI (200mV or 350mV Swing LVDS Selectable)
- Low Current Consumption for Mobile Application
- PLL requires no external components
- Package option: 4.5mm x 7mm BGA
  56-lead TSSOP(14mm X 8mm)
- Compatible with TIA/EIA-644 LVDS standard
- Compatible with SN75LVDS83B

Application

- Tablet PC, Media Tablet
- Mobile Internet Device
- Digital Picture Frame
- Smart Phone
- Mobile TV
- Netbook,
- Navigation
- Various Display Devices

Block Diagram



Option Pin Information

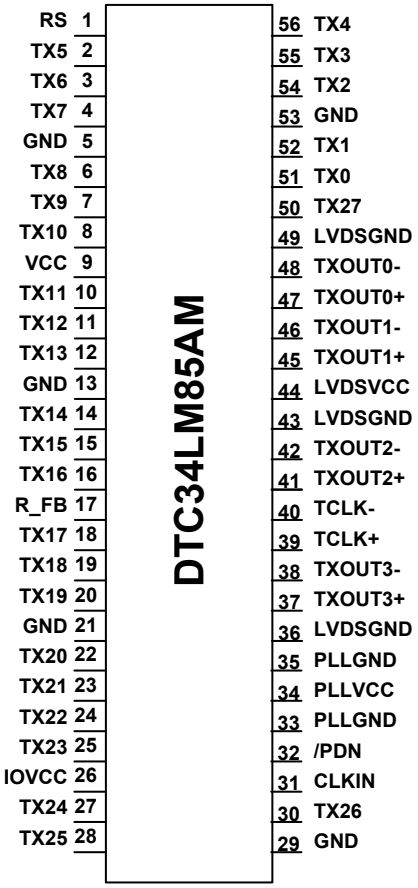
- The RS pin decides LVDS output swing level. (When The RS pin is 'IOVCC', LVDS output swing is 350mV)
- The R_FB pin decides clock edge of input signals. (When the R_FB pin is floating, falling edge is default.)
- The RSVD pin is not used for 24-bit color display. (If the RSVD is not used, it should be connected to GND)

Ordering Information

PART NUMBER	PART MARKING	PACKAGE
DTC34LM85AM	34LM85AM in BGA package	56-pin T&R
DTC34LM85AMT	34LM85AM in TSSOP package	56-pin T&R

TSSOP PIN OUT

(TOP VIEW)

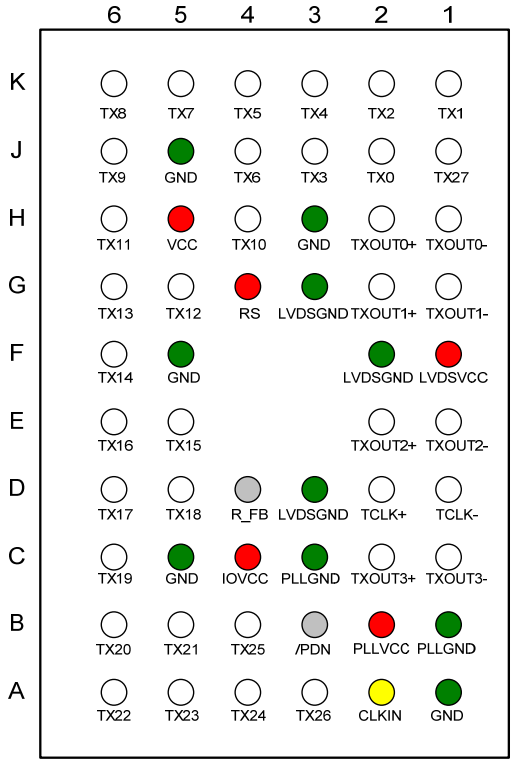


TSSOP PIN LIST

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	RS	15	TX15	29	GND	43	LVDSGND
2	TX5	16	TX16	30	TX26	44	LVDSVCC
3	TX6	17	R_FB	31	CLKIN	45	TXOUT1+
4	TX7	18	TX17	32	/PDN	46	TXOUT1-
5	GND	19	TX18	33	PLLGND	47	TXOUT0+
6	TX8	20	TX19	34	PLLVCC	48	TXOUT0-
7	TX9	21	GND	35	PLLGND	49	LVDSGND
8	TX10	22	TX20	36	LVDSGND	50	TX27
9	VCC	23	TX21	37	TXOUT3+	51	TX0
10	TX11	24	TX22	38	TXOUT3-	52	TX1
11	TX12	25	TX23	39	TCLK+	53	GND
12	TX13	26	IOVCC	40	TCLK-	54	TX2
13	GND	27	TX24	41	TXOUT2+	55	TX3
14	TX14	28	TX25	42	TXOUT2-	56	TX4

BGA PIN OUT

(TOP VIEW)



BGA PIN LIST

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	GND	A2	CLKIN	A3	TX26
A4	TX24	A5	TX23	A6	TX22
B1	PLLGND	B2	PLLVCC	B3	/PDN
B4	TX25	B5	TX21	B6	TX20
C1	TXOUT3-	C2	TXOUT3+	C3	PLLGND
C4	IOVCC	C5	GND	C6	TX19
D1	TCLK-	D2	TCLK+	D3	LVDSGND
D4	R_FB	D5	TX18	D6	TX17
E1	TXOUT2-	E2	TXOUT2+	E3	ball not populated
E4	ball not populated	E5	TX15	E6	TX16
F1	LVDSVCC	F2	LVDSGND	F3	ball not populated
F4	ball not populated	F5	GND	F6	TX14
G1	TXOUT1-	G2	TXOUT1+	G3	LVDSGND
G4	RS	G5	TX12	G6	TX13
H1	TXOUT0-	H2	TXOUT0+	H3	GND
H4	TX10	H5	VCC	H6	TX11
J1	TX27	J2	TX0	J3	TX3
J4	TX6	J5	GND	J6	TX9
K1	TX1	K2	TX2	K3	TX4
K4	TX5	K5	TX7	K6	TX8

Electrical Characteristics

Supply voltage DC SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Units
VCC	TTL input supply voltage	3.0	3.3	3.6	V
LVDSVCC	LVDS output supply voltage	3.0	3.3	3.6	V
PLLVCC	PLL supply voltage	3.0	3.3	3.6	V
IOVCC	IO supply voltage	1.62	1.8/2.5/3.3	3.6	V

CMOS/TTL DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	IOVCC=1.8V	IOVCC/2+0.3			V
		IOVCC=2.5V	IOVCC/2+0.4			
		IOVCC=3.3V	IOVCC/2+0.5			
V_{IL}	Low Level Input Voltage	IOVCC=1.8V			IOVCC/2-0.3	V
		IOVCC=2.5V			IOVCC/2-0.4	
		IOVCC=3.3V			IOVCC/2-0.5	
I_{IN}	Input Current	$0V \le V_{IN} \le$ IOVCC			±10	uA
I_{PD}	Pull Down Current	R_FB pin			10	uA

LVDS TRANSMITTER DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage, Normal RS= IOVCC (Small RS=GND, or DTC34LM85AMR)	RL=100Ω	250 (100)	350 (200)	450 (300)	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between Complimentary Output States				35	mV
I_{OZ}	Output TRI-STATE Current	/PDN=0V, Vout=0 to Vcc			±10	uA

TRANSMITTER SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{TG}	Transmitter Supply Current (16 Grayscale)	RL=100Ω, CL = 10pF, f = 85MHz RS= IOVCC (RS=GND,or DTC34LM85AMR)		47 (42)	mA
ICC_{TW}	Transmitter Supply Current (Worst Case)	RL=100Ω, CL = 10pF, f = 85MHz RS= IOVCC (RS=GND,or DTC34LM85AMR)		50 (45)	mA
ICC_{TP}	Transmitter Supply Current (Power Down)	/PDN=0V	10		uA

* All typical values are Vcc = 3.3V, Ta = 25°C

Absolute Maximum Ratings (Note1)

Supply Voltage (Vcc)	-0.3 to +4.0V
CMOS/TTL Input Voltage	-0.3V to (IOVCC + 0.3V)
CMOS/TTL Output Voltage	-0.3V to (Vcc + 0.3V)
LVDS Driver Output Voltage	-0.3V to (Vcc + 0.3V)
Output Short Circuit Duration	Continuous
Junction Temperature	+150 °C
Storage Temperature Range	-65 °C to 150 °C
Lead Temperature (Soldering, 4 sec.)	+260 °C
Maximum Power Dissipation @25°C	1.4W

(Note 1)

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation

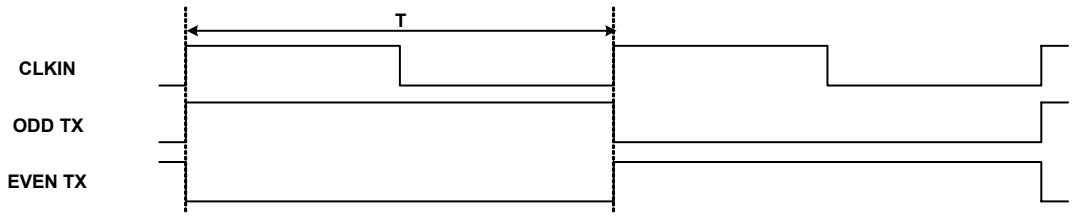
Transmitter Switching Characteristics

VCC=LVDSVCC=PLLVCC= 3.0~3.6V, IOVCC=1.62~3.6V, Ta=-10 ~ +70°C, T=1/f

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLKIN Transition Time			3.0	nS
t_{TCP}	CLKIN Period	7.4	T	50	nS
t_{TCH}	CLKIN High Time	0.4T	0.5T	0.6T	nS
t_{TCL}	CLKIN Low Time	0.4T	0.5T	0.6T	nS
t_{TCD}	CLKIN to TCLK+/- Delay		2T/7 + 2.3		nS
t_{TS}	TTL Data Setup to CLKIN	2.0			nS
t_{TH}	TTL Data Hold from CLKIN	2.0			nS
t_{LVT}	LVDS Transition Time		0.22	0.5	nS
t_{TDP1}	Transmitter Output Data Position 0 (135MHz)	-0.1	0	0.1	nS
t_{TDP0}	Transmitter Output Data Position 1 (135MHz)	T/7-0.1	T/7	T/7+0.1	nS
t_{TDP6}	Transmitter Output Data Position 2 (135MHz)	2T/7-0.1	2T/7	2T/7+0.1	nS
t_{TDP5}	Transmitter Output Data Position 3 (135MHz)	3T/7-0.1	3T/7	3T/7+0.1	nS
t_{TDP4}	Transmitter Output Data Position 4 (135MHz)	4T/7-0.1	4T/7	4T/7+0.1	nS
t_{TDP3}	Transmitter Output Data Position 5 (135MHz)	5T/7-0.1	5T/7	5T/7+0.1	nS
t_{TDP2}	Transmitter Output Data Position 6 (135MHz)	6T/7-0.1	6T/7	6T/7+0.1	nS
t_{TPLLS}	Transmitter Phase Lock Loop Set	-	-	10	mS

AC Timing Diagrams

FIGURE 1. Test Pattern “Worst Case Pattern”



AC Timing Diagrams(Continued)

FIGURE 2. Test Pattern "16 Grayscale Test Pattern"

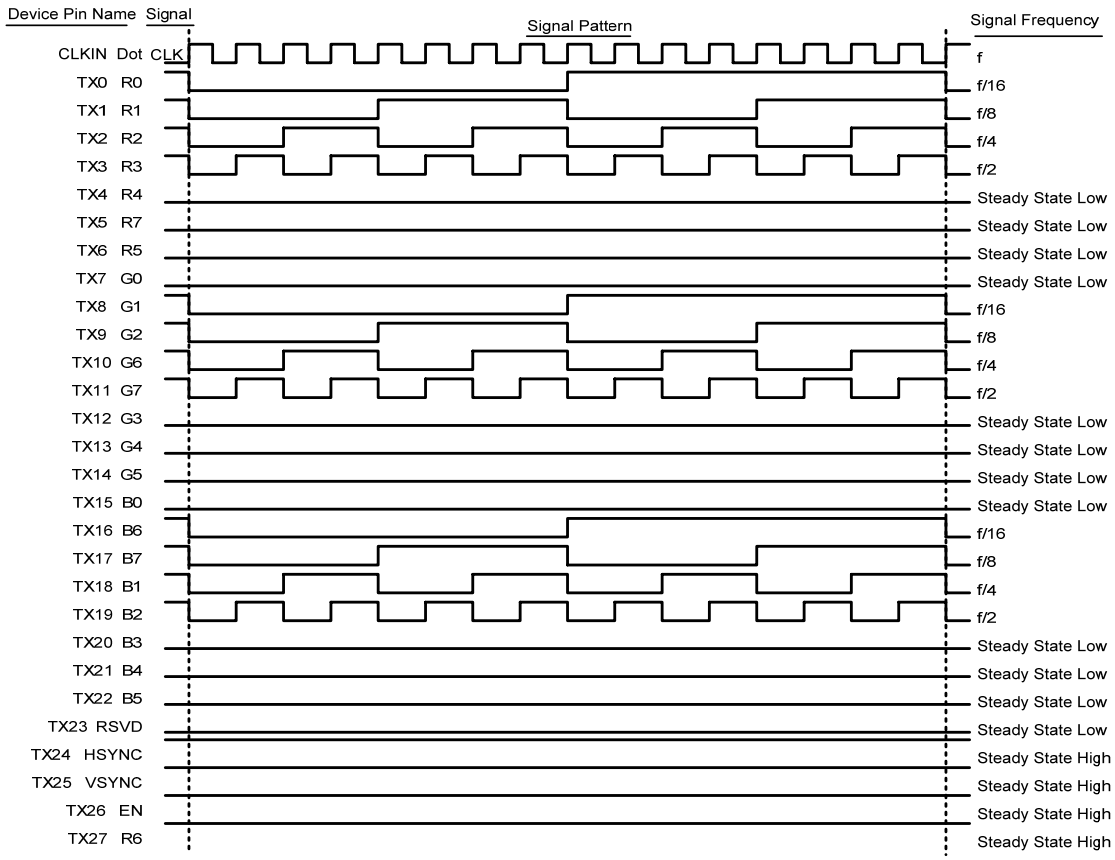


FIGURE 3. TTL Input

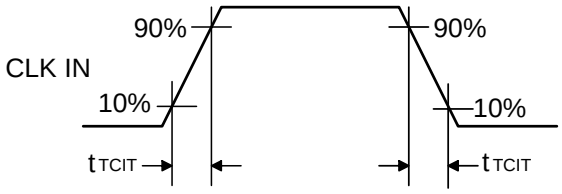
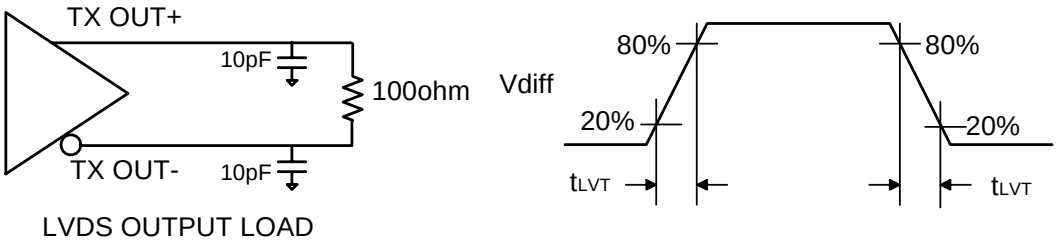


FIGURE 4. LVDS Output

Vdiff= (TXOUT+) – (TXOUT–)



AC Timing Diagrams (Continued)

FIGURE 5. Phase Lock Loop Set Time

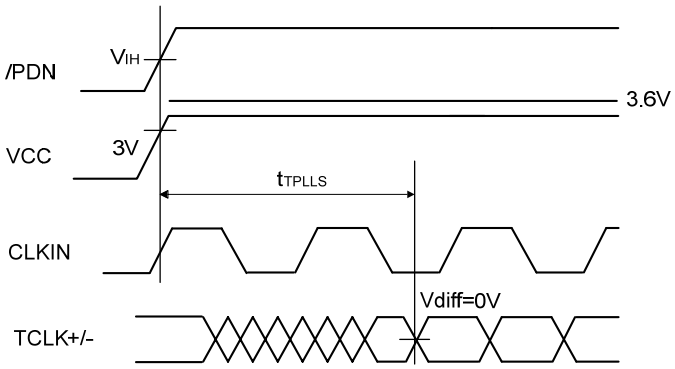
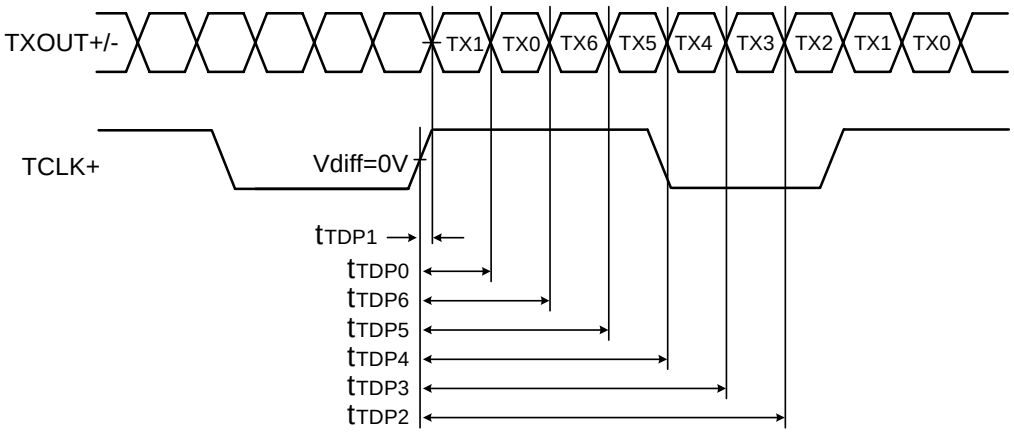


FIGURE 6. Transmitter Device Operation



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) – (TCLK-)**

FIGURE 7. Parallel TTL Data Inputs Mapped to LVDS Outputs – DTC34LM85AM

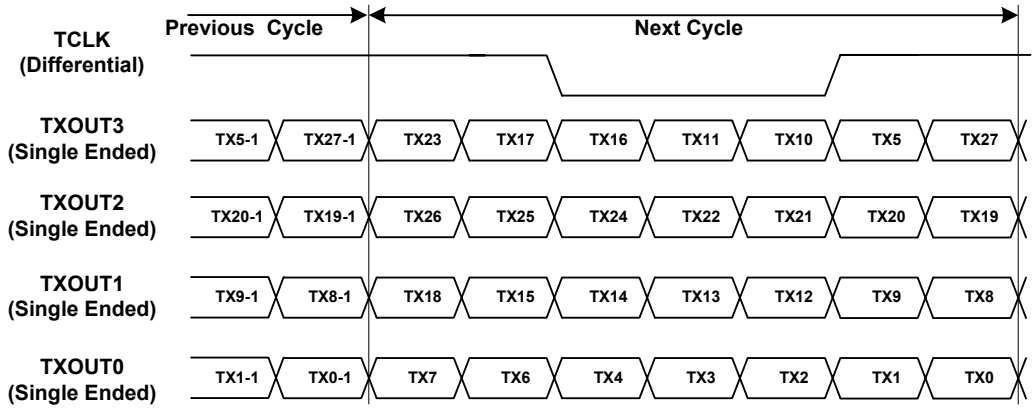
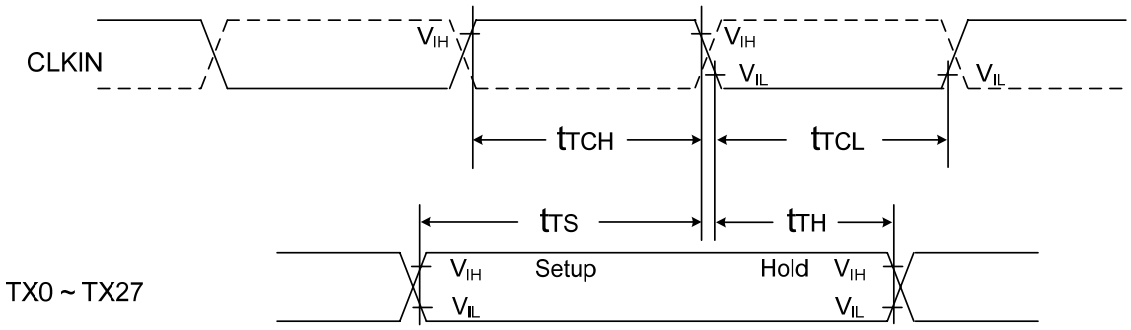


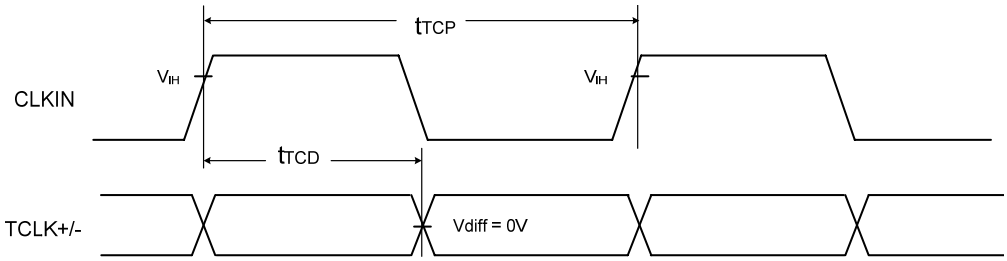
FIGURE 8. Setup/Hold and High/Low Times



Note : **1) CLKIN : for DTC34LM85AM(R_FB=GND), denoted as solid line**

for DTC34LM85AM(R_FB= IOVCC), denoted as dotted line

FIGURE 9. CLKIN to CLKOUT Delay

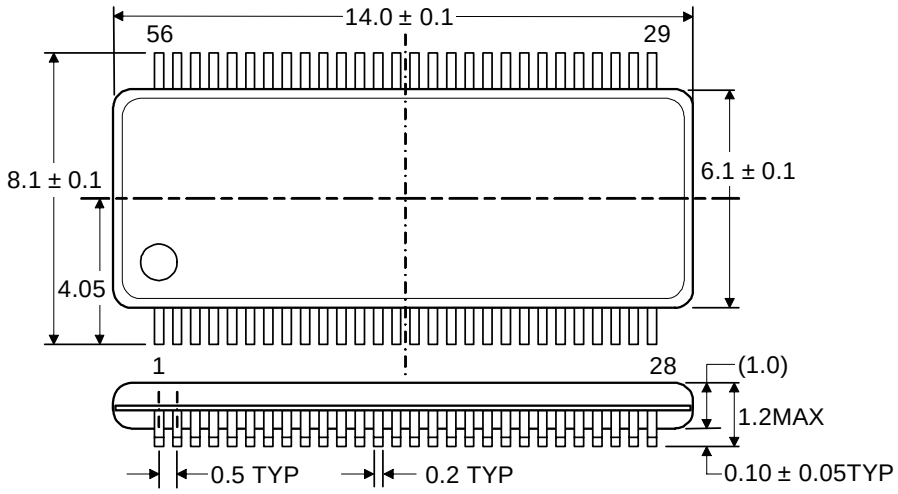


Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) - (TCLK-)**

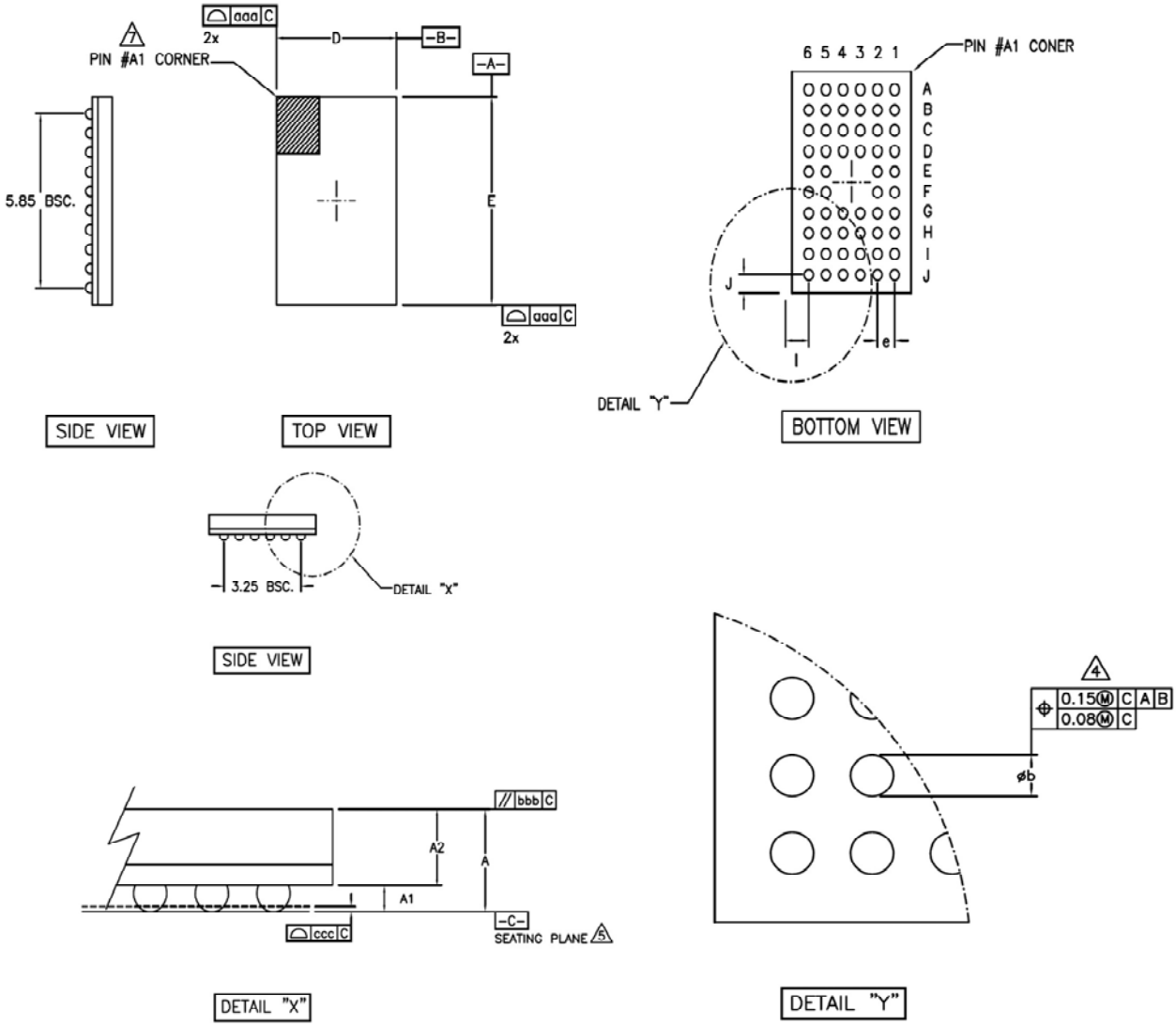
TSSOP PACKAGE

56 Lead Molded Thin Shrink Small Outline Package, JEDEC

Unit : millimeters



BGA PACKAGE



SYMBOL	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.15	0.18	0.21
A2	0.71	0.75	0.79
D	4.40	4.50	4.60
E	6.90	7.00	7.10
I	0.625 REF.		
J	0.575 REF.		
M	6X10		
aaa			0.10
bbb			0.10
ccc			0.10
b	0.35	0.40	0.45
e	0.65 TYP.		

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DEMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C .
5. PRIMARY DATUM C AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
7. A1 CORNER MUST BE IDENTIFIED BY LASER MARK.

APPLICATION INFORMATION

This application note's purpose is not to specify a strict circuit implementation of a display system using the DTC FPD Interface chipset family, but to provide some guidelines for successful implementation of it.

System Designing Considerations

PCB Layout Considerations

Lines of a LVDS differential signal pair should always be adjacent to eliminate noise interference from other signals and effectively cancel the noise on the differential signals.

The physical length of PCB trace for a given LVDS differential signal pair should be matched as much as possible.

The physical length of PCB trace for each LVDS differential signal pairs should be keep as short as possible; otherwise the differential impedance of PCB must be controlled to be near 100 Ohm.

The physical length of PCB trace of CMOS/TTL signals should be keep as short and close to the same as possible. The PCB trace of CMOS/TTL signals should be isolated from LVDS differential signal pairs, placing them at least "3s" or "2w" away (see Figure 10).

To limit the impedance discontinuities causing signal reflection and crosstalk, the 90° angle on PCB trace must be not used (see Figure 11) and the number of via should be reduced.

If any impedance discontinuities occur on one signal line, it must be mirrored in the other line of the differential pair.

These considerations reduce the signal reflection and crosstalk, and make it helpful to obtain full benefit of the noise and EMI reduction from LVDS.

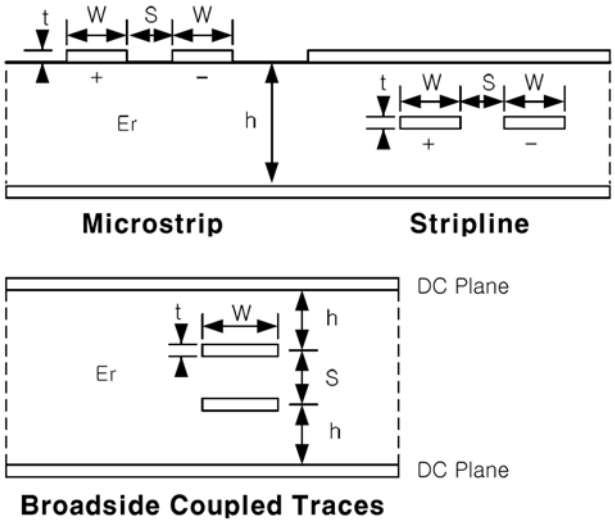


Figure10. PCB Construct Cross-section

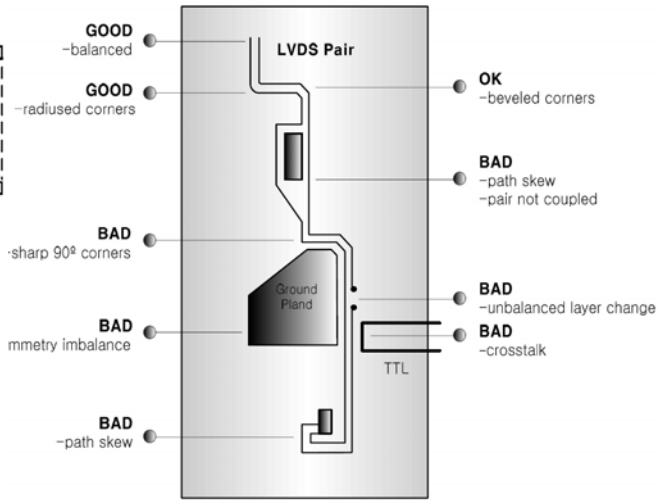


Figure11. PCB Layout Example

Termination

Because of using current mode output driver in LVDS, a termination resistor is required across the receiver's differential input pair per channel and its typical value is 100 Ohms (see Figure 12).

These termination resistors should be placed as close as possible to the receiver's input pins to shorten stubs and effectively terminate the differential lines.

For the type of resistor, surface mount resistors are recommended rather than leaded resistors to avoid additional parasitic inductance.

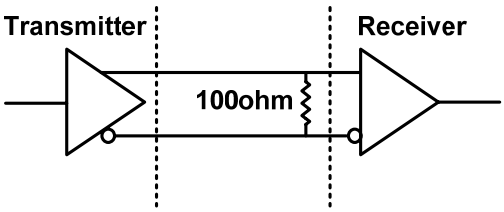


Figure12. LVDS Differential Termination

Power & Ground

Power supply system performance can be greatly improved by bypassing capacitors that reduce the impact of switching noise and its feedback or interference between different blocks of the circuits.

In general, each VCC pins are required to have separate bypassing sufficient to ensure less than 100 mV peak-to-peak noises on the supply pins, especially PVCC.

Power Up Sequencing

A specific power up sequence is not required in the DTC FPD Interface chipset family. But the best practice is: power up all VCC together, apply clocks, and then assert /PDN power-down pins high to enable the transmitter and/or receiver.

The /PDN pin is internally pulled down to ground that the device is disabled if this pin is left open circuited.

When powering down the device, the transmitter outputs remain in tri-state and the receiver outputs are low.

When the device are actively driven, the /PDN pin should be pulled up to VCC by no more than a 10 kOhms resistor.

Falling edge or Rising edge Selection

The DTC FPD receivers are available with either a falling edge data strobe or a rising edge data strobe, which is selectable according to the LCD panel timing controller requirements. The strobe edge only affects the TTL inputs of the transmitter or outputs of the receiver, while the LVDS interface is not affected.

Bit Mapping of FPD Interface Data

The transmitter's data input from the graphic controller consist of 18 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, and an enable bit for 18-bit device, or consist of 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit , and a spare bit for 24-bit device. Only three LVDS data channels are required for and 18-bit FPD interface application.

The most significant bits (MSB) for an 18-bit application must be mapped exactly the same as the most significant bits in the 24-bit application, and additional least significant in the 24-bit application are mapped the 4th LVDS data channel.

The output of the receiver to LCD panel controller has same bit mapping as the input to the transmitter.

The detailed bit mapping information between the RGB data of graphic information and the CMOS/TTL data pins of the transmitter/receiver is listed in Table 1, and that between the data arrangement of LVDS channels and the CMOS/TTL data pins of the transmitter/receiver is also described in Figure 13 and Figure 14.

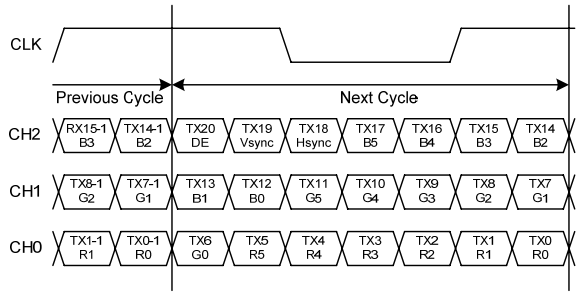


Figure13. Bit Mapping between LVDS and CMOS/TTL signals for 18-bit Color Display

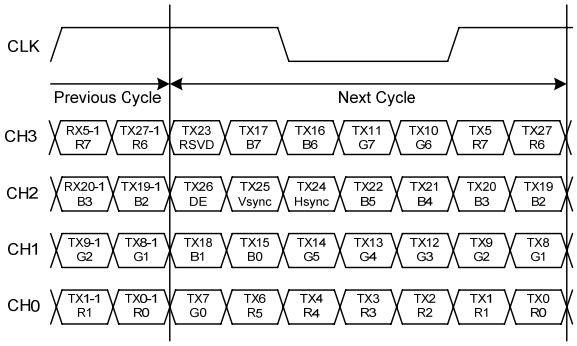


Figure14. Bit Mapping between LVDS and CMOS/TTL signals for 24-bit Color Display

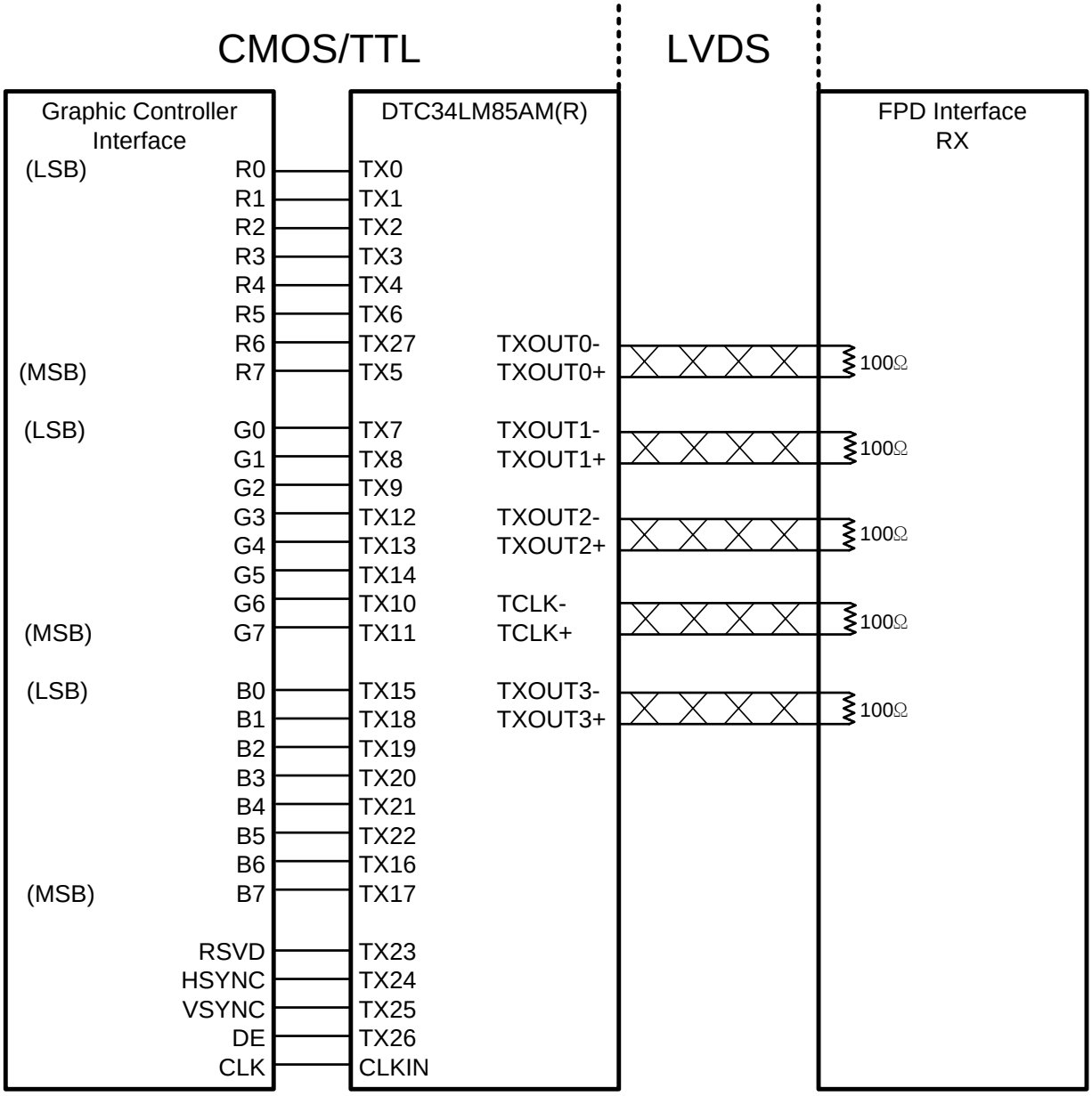


Figure15. 24bit FPD interface Application

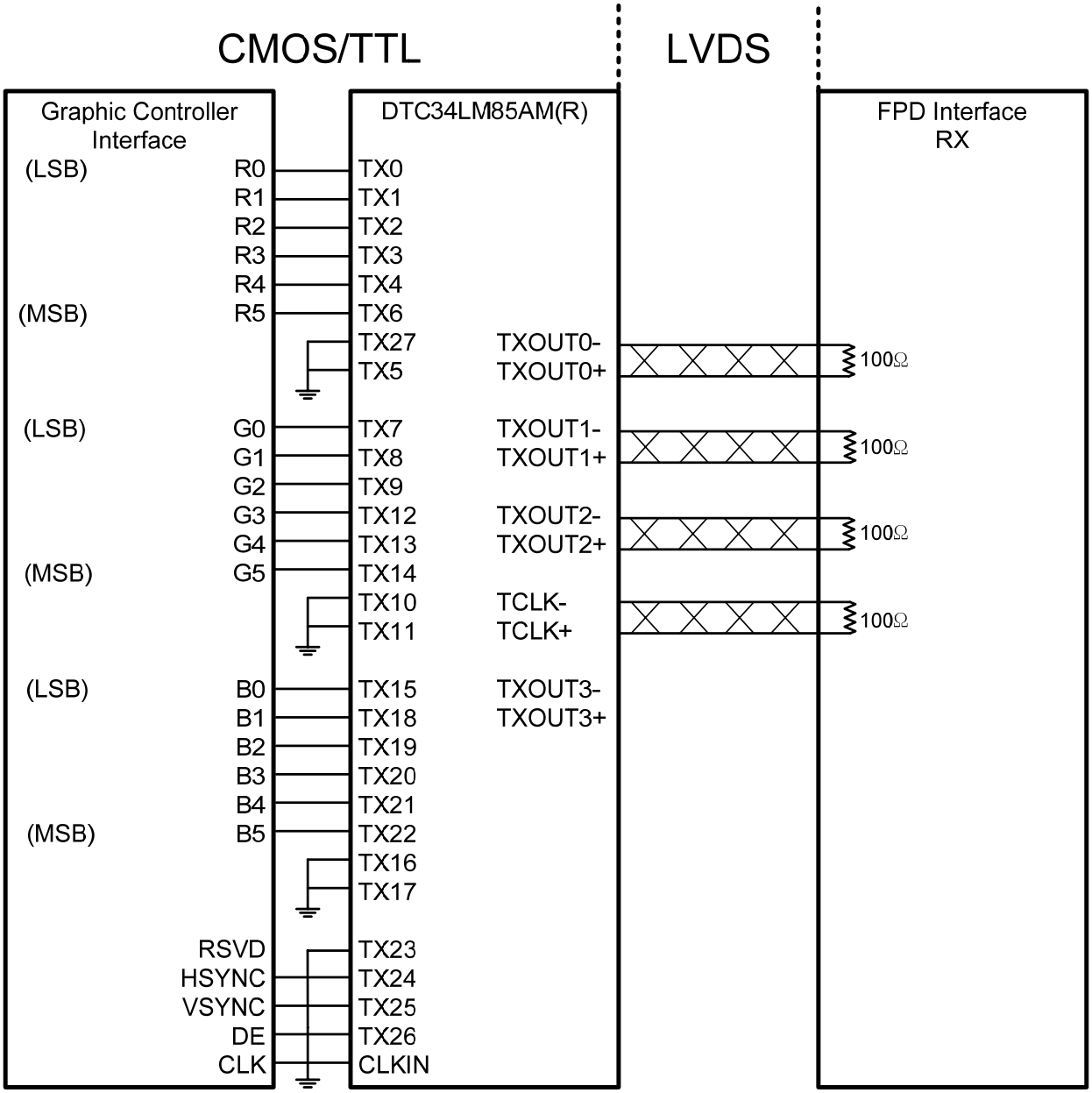


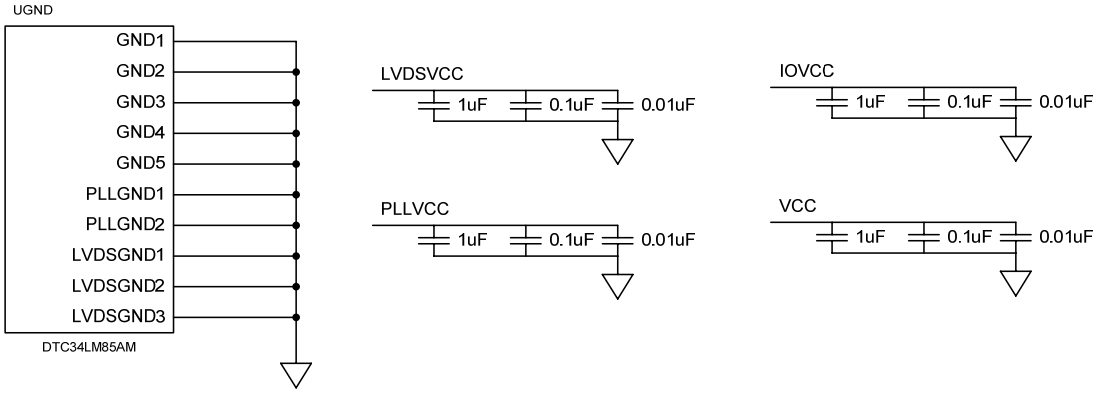
Figure16. 18bit FPD interface Application

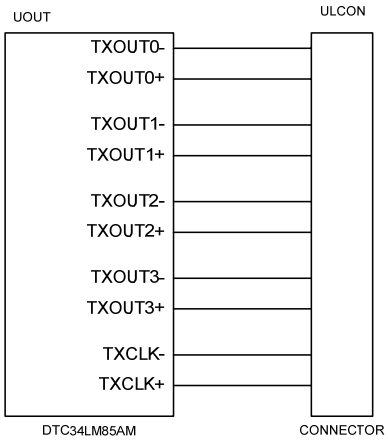
Bit Mapping for 18-bit and 24-bit Color Display

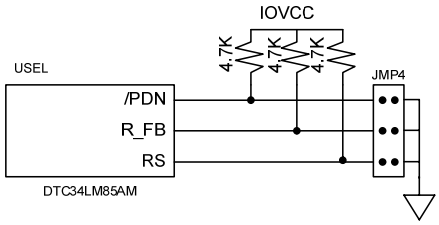
VGA-TFT Data Signal			Transmitter Input Data Pin		Receiver Output Data Pin		TFT Panel Data Signal	
	24-bit	18-bit	24-bit Tx (34LM85)	18-bit Tx (33LM85)	24-bit Rx (34LF/LR86)	18-bit Rx (33LF/LR86)	18-bit	24-bit
LSB	R0		TX0		RX0			R0
	R1		TX1		RX1			R1
	R2	R0	TX2	TX0	RX2	RX0	R0	R2
	R3	R1	TX3	TX1	RX3	RX1	R1	R3
	R4	R2	TX4	TX2	RX4	RX2	R2	R4
	R5	R3	TX6	TX3	RX6	RX3	R3	R5
	R6	R4	TX27	TX4	RX27	RX4	R4	R6
MSB	R7	R5	TX5	TX5	RX5	RX5	R5	R7
LSB	G0		TX7		RX7			G0
	G1		TX8		RX8			G1
	G2	G0	TX9	TX6	RX9	RX6	G0	G2
	G3	G1	TX12	TX7	RX12	RX7	G1	G3
	G4	G2	TX13	TX8	RX13	RX8	G2	G4
	G5	G3	TX14	TX9	RX14	RX9	G3	G5
	G6	G4	TX10	TX10	RX10	RX10	G4	G6
MSB	G7	G5	TX11	TX11	RX11	RX11	G5	G7
LSB	B0		TX15		RX15			B0
	B1		TX18		RX18			B1
	B2	B0	TX19	TX12	RX19	RX12	B0	B2
	B3	B1	TX20	TX13	RX20	RX13	B1	B3
	B4	B2	TX21	TX14	RX21	RX14	B2	B4
	B5	B3	TX22	TX15	RX22	RX15	B3	B5
	B6	B4	TX16	TX16	RX16	RX16	B4	B6
MSB	B7	B5	TX17	TX17	RX17	RX17	B5	B7
	RSVD		TX23		RX23			RSVD
	Hsync	Hsync	TX24	TX18	RX24	RX18	Hsync	Hsync
	Vsync	Vsync	TX25	TX19	RX25	RX19	Vsync	Vsync
	DE	DE	TX26	TX20	RX26	RX20	DE	DE

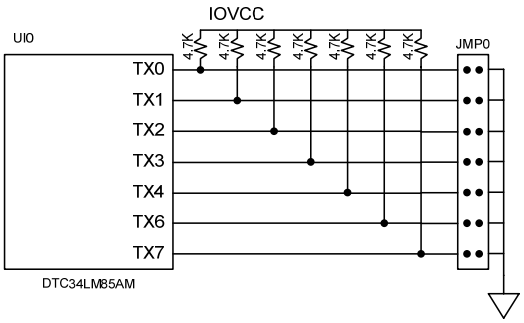
Table1. Bit Mapping for 18bit and 24bit Color Display.

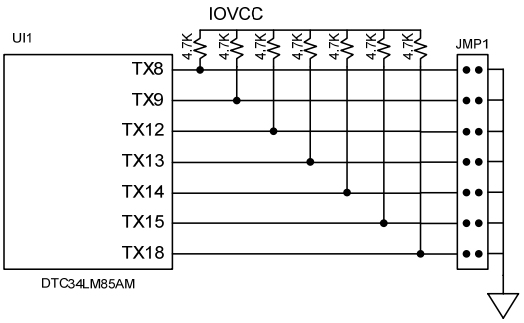
Typical Application Schematic

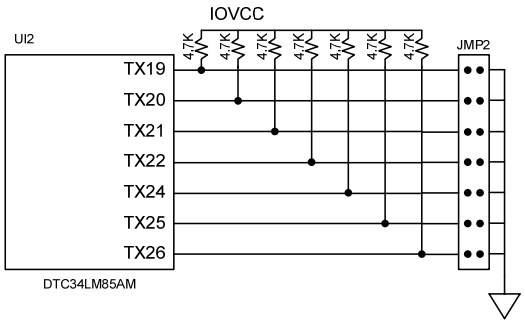


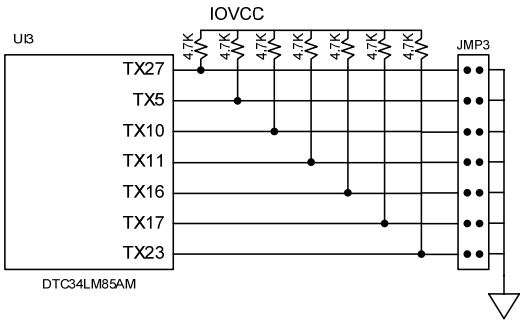












Pin Name	Pin # (TSSOP)	Pin #(BGA)	Type	Description
TXOUT0-, TXOUT0+	48, 47	H1,H2	LVDS OUT	LVDS differential data outputs.
TXOUT1-, TXOUT1+	46, 45	G1,G2	LVDS OUT	
TXOUT2-, TXOUT2+	42, 41	E1,E2	LVDS OUT	
TXOUT3-, TXOUT3+	38, 37	C1,C2	LVDS OUT	
TCLK-, TCLK+	40, 39	D1,D2	LVDS OUT	LVDS differential clock outputs.
TX0 ~ TX6	51,52,54,55,56,2, 3	J1,K1,K2,J3,K3,K4,J4	IN	Data inputs. This includes : 8 Red, 8 Green, 8 Blue, and 3 control lines (HSYNC, VSYNC, DE) and 1 RSVD
TX7 ~ TX13	4,6,7,8,10,11,12	K5,K6,J6,H4,H6,G5,G6	IN	
TX14 ~ TX20	14,15,16,18,19,20,22	F6,E5,E6,D6,D5,C6,B6	IN	
TX21 ~ TX27	23,24,25,27,28,30,50	B5,A6,A5,A4,B4,A3,J1	IN	
CLKIN	31	A2	IN	Clock input. This falling edge acts as data strobe
/PDN	32	B3	IN	Power down control /PDN=IOVCC : Normal operation /PDN=GND : Power down (all output are low)
R_FB	17	D4	IN	Programmable strobe select. R_FB=IOVCC :Rising edge, R_FB=GND:Falling edge
RS	1	G4	IN	LVDS Swing Control (Normal RS=IOVCC, Small RS=GND) DTC34LM85AMR = Don't care pin
VCC	9	H5	Power	Power supply pins for digital.
GND	5,13,21,29,53	A1,C5,F5,H3,J5	Ground	Ground pins for digital.
LVDSVCC	44	F1	Power	Power supply pin for LVDS outputs.
LVDSGND	36,43,49	D3,F2,G3	Ground	Ground pins for LVDS outputs.
PLLVCC	34	B2	Power	Power supply pin for PLL.
PLLGND	33,35	B1,C3	Ground	Ground pin for PLL.
IOVCC	26	C4	Power	Power pin for IO.

Table2. Package Pin Description

IMPORTANT NOTICE:

- The contents of this data sheet are subject to change without prior notice.

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