LVDS Product

# DTC33LF86L/ DTC33LR86L (*Rev. 2.2*)

*REVISED APR. 2009*

## +3.3V LVDS 18Bit Flat Panel Display (FPD) Receiver - 85MHz

### General Description

The DTC33LF86L/DTC33LR86L receivers convert the LVDS (Low Voltage Differential Signaling) data streams back into 21 bits of CMOS/TTL data with falling edge (DTC33LF86L) or rising edge (DTC33LR86L) clock for convenient interface with a variety of LCD panel controllers.

A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. A transmitter (DTC33LM85AL) will inter-operate with a Falling / Rising edge receiver (DTC33LF86L / LR86L) without any translation logic.

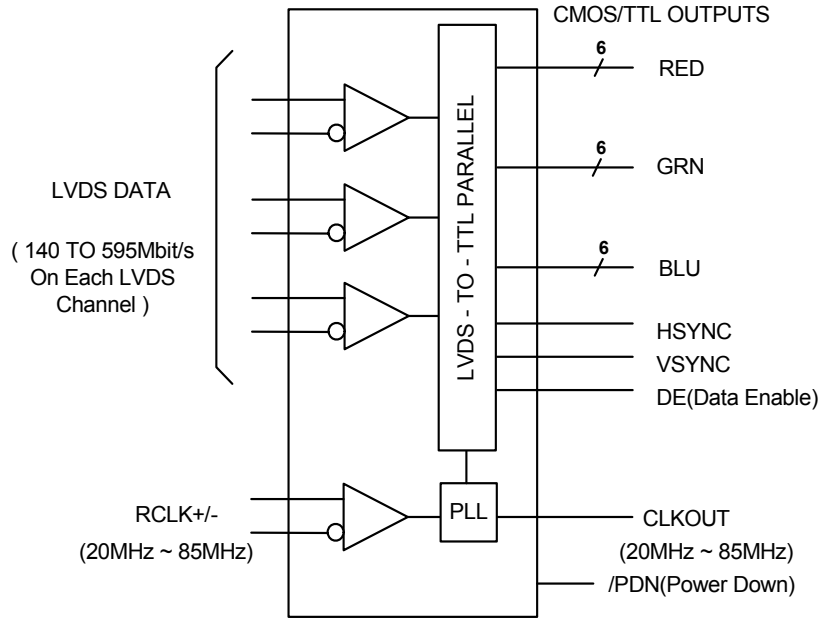
Using a 85 MHz clock, the data throughputs is 223 Mbytes/sec. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

### Features

- Wide frequency range : 20 to 85 MHz shift clock support
- Narrow bus (8 lines) reduces cable size
- Single 3.3V supply
- Power-Down Mode
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and SXGA
- Up to 223 Megabytes/sec bandwidth
- Up to 1.78 Gbps throughput
- 300mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 48-lead TSSOP package (PB Free)
- Compatible with TIA/EIA-644 LVDS standard
- Compatible with the National DS90C366, Thine THC63LVDF64A

## Block Diagram

**DTC33LF86L/DTC33LR86L**



# Electrical Characteristics

**Vcc=3.0 ~ 3.6V @ Ta=-10 ~ +70°C**

## CMOS/TTL DC SPECIFICATIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | Vcc | V |
| $V_{IL}$ | Low Level Input Voltage | | GND | | 0.8 | V |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = -4mA | 2.4 | | | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = 4mA | | | 0.4 | V |
| $I_{IN}$ | Input Current | 0V ≤ $V_{IN}$ ≤ Vcc | | | ±10 | uA |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V | | | -50 | mA |

## LVDS RECEIVER DC SPECIFICATIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{TH}$ | Differential Input High Threshold | $V_{OC}$= +1.2V | | | +100 | mV |
| $V_{TL}$ | Differential Input Low Threshold | | -100 | | | mV |
| $I_{IN}$ | Input Current | $V_{IN}$= +2.4V/0V, Vcc= 3.6V | | | ±10 | uA |

## RECEIVER SUPPLY CURRENT

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $ICC_{RG}$ | Receiver Supply Current (16 Grayscale) | CL = 8pF, f = 85MHz, Vcc = 3.6V 16 Grayscale Pattern | 55 | | mA |
| $ICC_{RW}$ | Receiver Supply Current (Worst Case) | CL = 8pF, f = 85MHz, Vcc = 3.6V Worst Case Pattern | 80 | | mA |
| $ICC_{RP}$ | Receiver Supply Current (Power Down) | /PDN=0V | 10 | | uA |

### Absolute Maximum Ratings (Note1)

Supply Voltage (Vcc) -0.3 to +4.0V
CMOS/TTL Input Voltage -0.3V to (Vcc + 0.3V)
CMOS/TTL Output Voltage -0.3V to (Vcc + 0.3V)
LVDS Driver Output Voltage -0.3V to (Vcc + 0.3V)
Output Short Circuit Duration Continuous
Junction Temperature +150°C
Storage Temperature Range –65°C to 150°C
Lead Temperature (Soldering, 4 sec.) +260°C
Maximum Power Dissipation @25°C 1.4W

**(Note 1)**

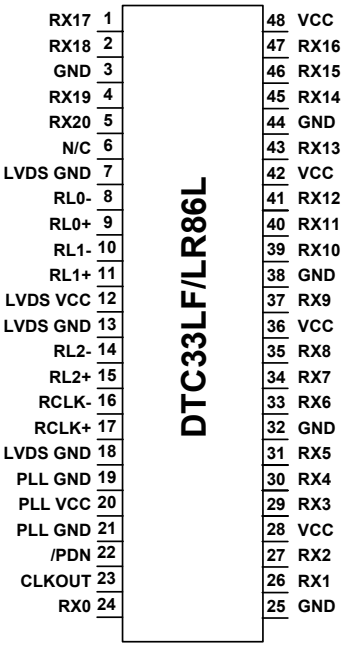
"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation

## Receiver Switching Characteristics

**Vcc=3.0 ~ 3.6V Ta=-10 ~ +70°C, T=1/f**

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{RCP}$ | CLKOUT Period | 11.76 | T | 50 | nS |
| $t_{RCH}$ | CLKOUT High Time | 4.5 | 5.0 | 7.0 | nS |
| $t_{RCL}$ | CLKOUT Low Time | 4.0 | 5.0 | 6.5 | nS |
| $t_{RCD}$ | RCLK+/- to CLKOUT Delay | | 7.0 | | nS |
| $t_{RS}$ | TTL Data Setup to CLKOUT | 3.5 | | | nS |
| $t_{RH}$ | TTL Data Hold from CLKOUT | 3.5 | | | nS |
| $t_{TLH}$ | TTL Low to High Transition Time | | 3 | | nS |
| $t_{THL}$ | TTL High to Low Transition Time | | 3 | | nS |
| $t_{RDP5}$ | Receiver Input Data Position 0 (85MHz) | -0.4 | 0 | 0.4 | nS |
| $t_{RDP6}$ | Receiver Input Data Position 1 (85MHz) | T/7-0.4 | T/7 | T/7+0.4 | nS |
| $t_{RDP0}$ | Receiver Input Data Position 2 (85MHz) | 2T/7-0.4 | 2T/7 | 2T/7+0.4 | nS |
| $t_{RDP1}$ | Receiver Input Data Position 3 (85MHz) | 3T/7-0.4 | 3T/7 | 3T/7+0.4 | nS |
| $t_{RDP2}$ | Receiver Input Data Position 4 (85MHz) | 4T/7-0.4 | 4T/7 | 4T/7+0.4 | nS |
| $t_{RDP3}$ | Receiver Input Data Position 5 (85MHz) | 5T/7-0.4 | 5T/7 | 5T/7+0.4 | nS |
| $t_{RDP4}$ | Receiver Input Data Position 6 (85MHz) | 6T/7-0.4 | 6T/7 | 6T/7+0.4 | nS |
| $t_{RPLLS}$ | Receiver Phase Lock Loop Set | | | 10 | mS |

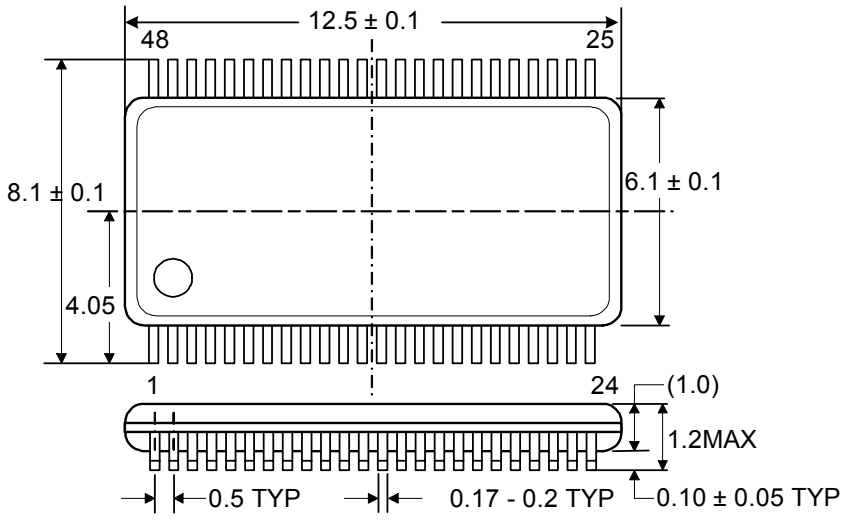
### PIN OUT




### PACKAGE

48 Lead Molded Thin Shrink Small Outline Package, JEDEC

Unit : millimeters



# AC Timing Diagram

**FIGURE 1. Test Pattern "16 Grayscale Test Pattern"**

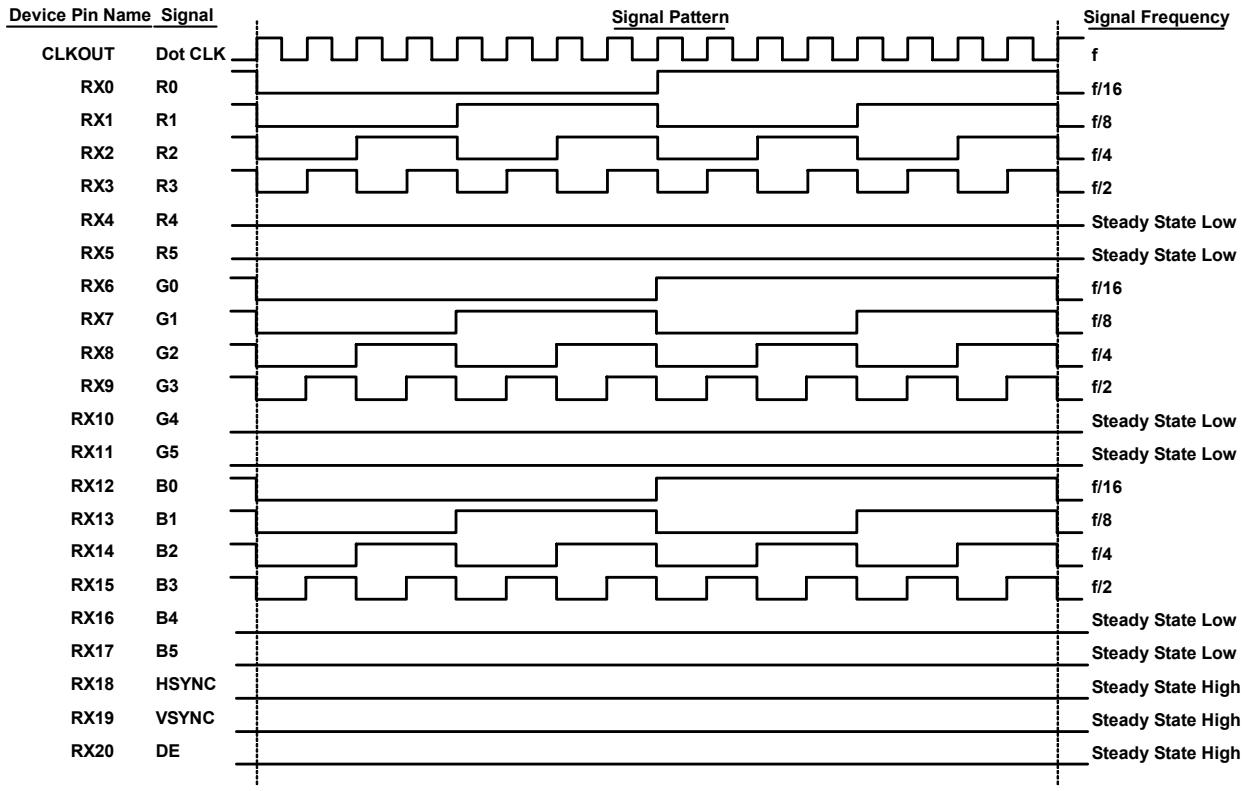



**FIGURE 2. Test Pattern "Worst Case Pattern"**

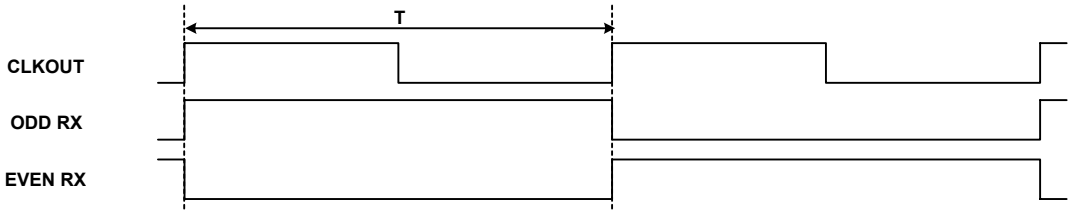
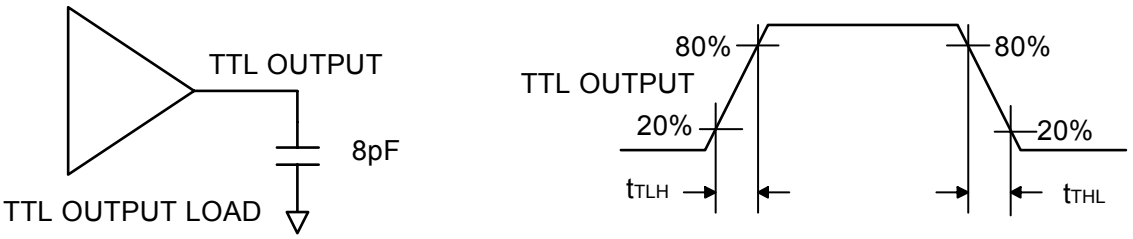



**FIGURE 3. TTL Output**



# AC Timing Diagram (Continued)

**FIGURE 4. Phase Lock Loop Set Time**

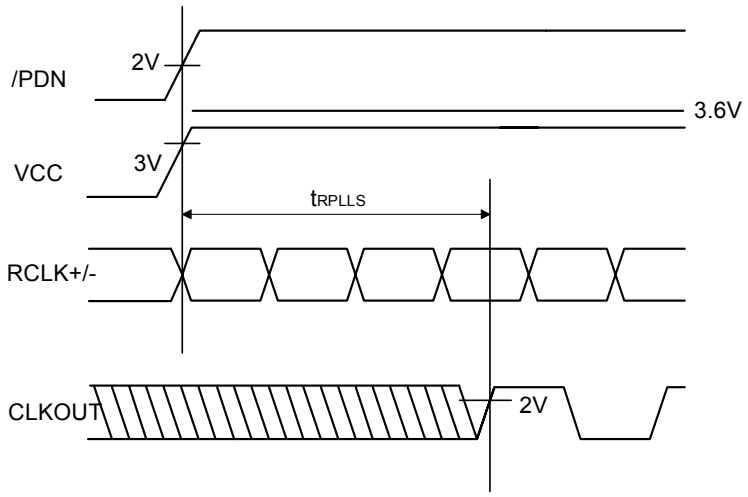
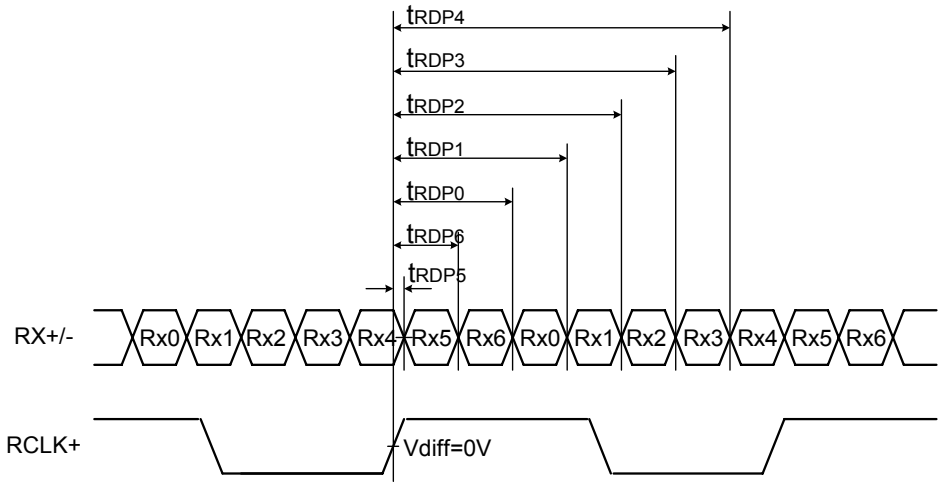



**FIGURE 5. Receiver Device Operation**




**Note** : **1) Vdiff = (RL+) - (RL-), .... (RCLK+) - (RCLK-)**

**FIGURE 6. LVDS Inputs Mapped Parallel TTL Data Outputs – DTC33LF86L/DTC33LR86L**

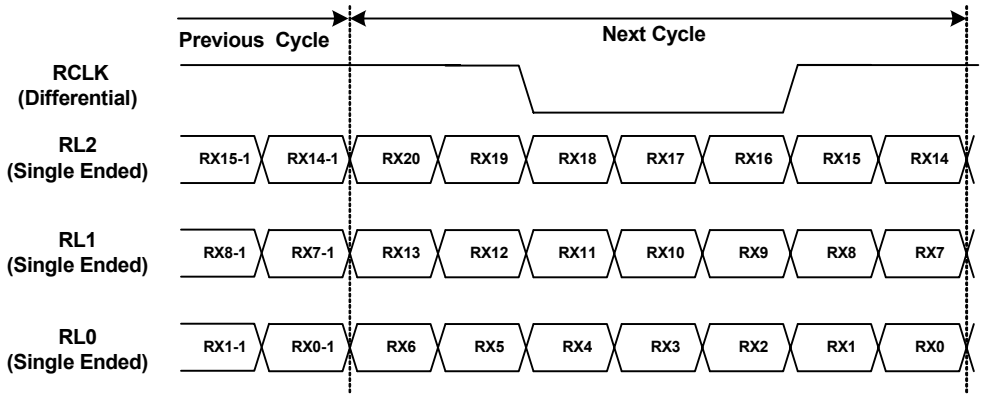
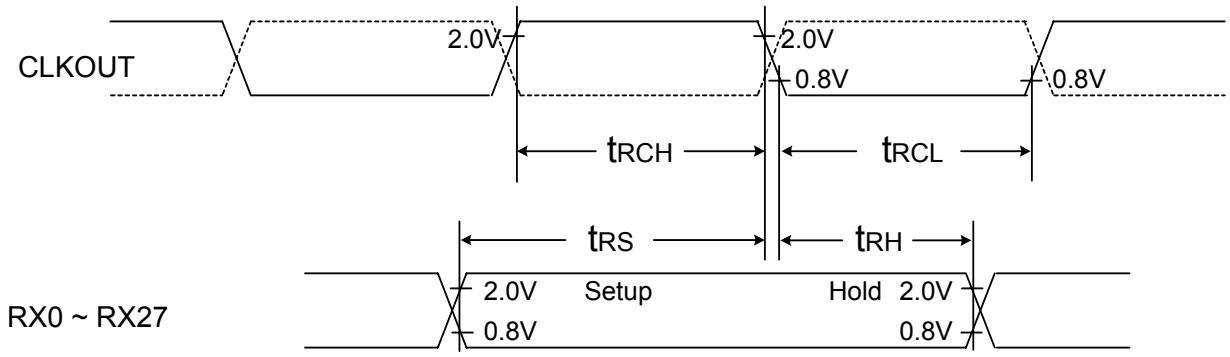
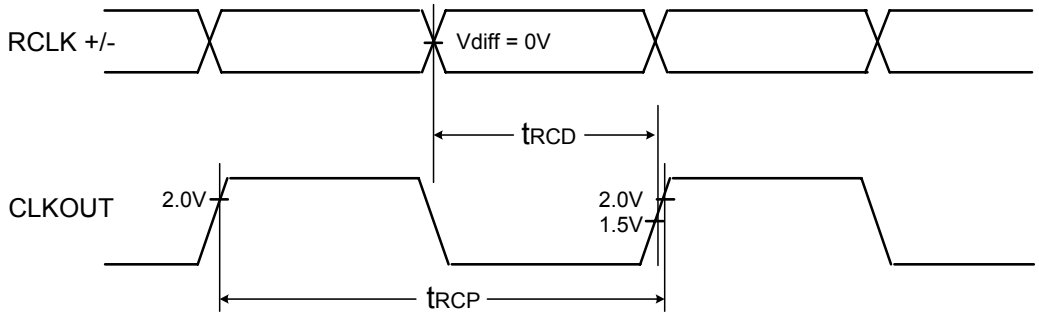



**FIGURE 7. Setup/Hold and High/Low Times**




**Note** : **1) CLKOUT for DTC33LF86L, denoted as solid line(dotted line is for DTC33LR86L)**,

**FIGURE 8. RCLK to CLKOUT Delay**




**Note** : **1) Vdiff = (RL+) - (RL-), .... (RCLK+) - (RCLK-)**

## FIGURE 9. Package Pin Description

| Pin Name | Pin # | Type | Description |
|---|---|---|---|
| RL0+,RL0- | 8, 9 | LVDS IN | LVDS differential data inputs. |
| RL1+, RL1- | 10, 11 | LVDS IN | |
| RL2+, RL2- | 14, 15 | LVDS IN | |
| RCLK+, RCLK- | 16, 17 | LVDS IN | LVDS differential clock inputs. |
| RX0 ~ RX6 | 24,26,27,29,30,31,33 | OUT | TTL level data outputs.<br>This includes : 6 Red, 6 Green, 6 Blue, and 3 control lines (HSYNC, VSYNC, DE) |
| RX7 ~ RX13 | 34,35,37,39,40,41,43 | OUT | |
| RX14 ~ RX20 | 45,46,47,1,2,4,5 | OUT | |
| CLKOUT | 23 | OUT | TTL level clock output. This falling edge acts as data strobe |
| /PDN | 22 | IN | TTL level input. H : Normal operation<br>L : Power down (all output are low) |
| VCC | 28,36,42,48 | Power | Power supply pins for TTL outputs. |
| GND | 3,25,32,38,44 | Ground | Ground pins for TTL outputs. |
| LVDS VCC | 12 | Power | Power supply pin for LVDS inputs. |
| LVDS GND | 7,13,18 | Ground | Ground pins for LVDS inputs. |
| PLL VCC | 20 | Power | Power supply for PLL. |
| PLL GND | 19,21 | Ground | Ground pin for PLL. |

## IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.

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