LVDS Product

DTC LVDS Products Application Note (*Preliminary Ver. 1.0*)

LVDS Flat Panel Display (FPD) Interface Transmitter/Receiver - 135MHz

Introduction

The DTC FPD Interface chipsets are the family of flat panel display system's interface devices specially configured to provide high-quality data transmission between graphic controller and LCD panels with high speed, low power and low EMI considerations as well as simpler physical interface concern. For these purpose, the DTC FPD Interface chipset family employs the LVDS (Low Voltage Differential Signaling) technology and offers better efficient method for high-end FPD system such as 1080p and QXGA resolution.

This application note's purpose is not to specify a strict circuit implementation of a display system using the DTC FPD Interface chipset family, but to provide some guidelines for successful implementation of it.

System Description

The example of typical display system using the DTC FPD interface chipset family is consist of transmitters and receivers (see Figure 1), interconnected over a cable including 3 to 10 twisted-pair data signal wires, one or two twisted-pair clock signal wires, a power wire and a ground wire. The DTC FPD interface chipset family includes devices to support 18-bit, 24-bit, 30bit and 60-bit color displays, a frequency range of 10 MHz to 135 MHz, and alternative selection of rising or falling edge for data and control strobe (see Figure 2).

Note: For more detailed information about the DTC FPD interface chipset, see the data sheets for DTC30LM35 and DTC30LM36

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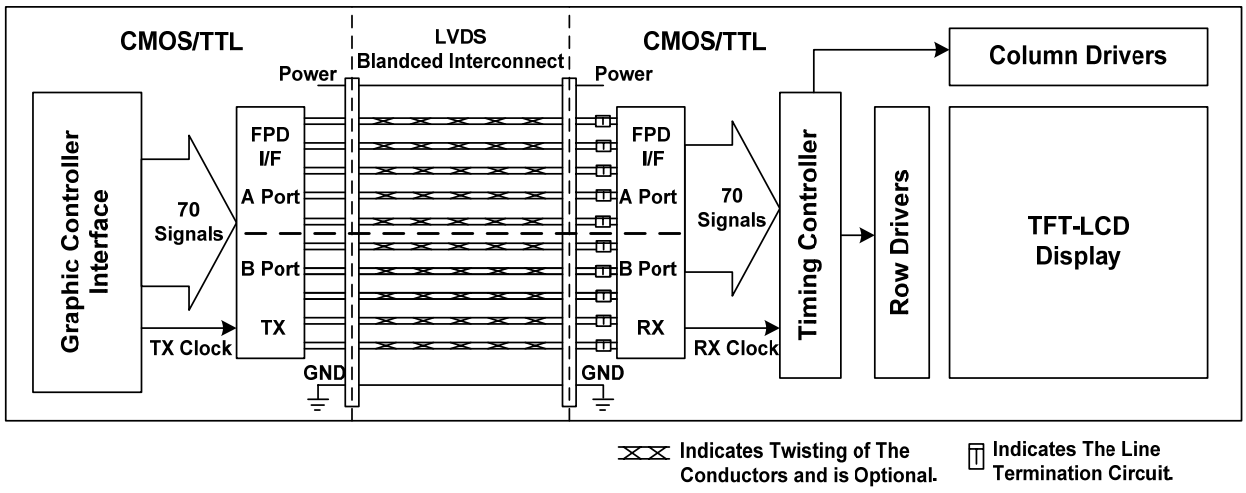

Figure 1. Typical FPD Link Application (60-Bit Color)

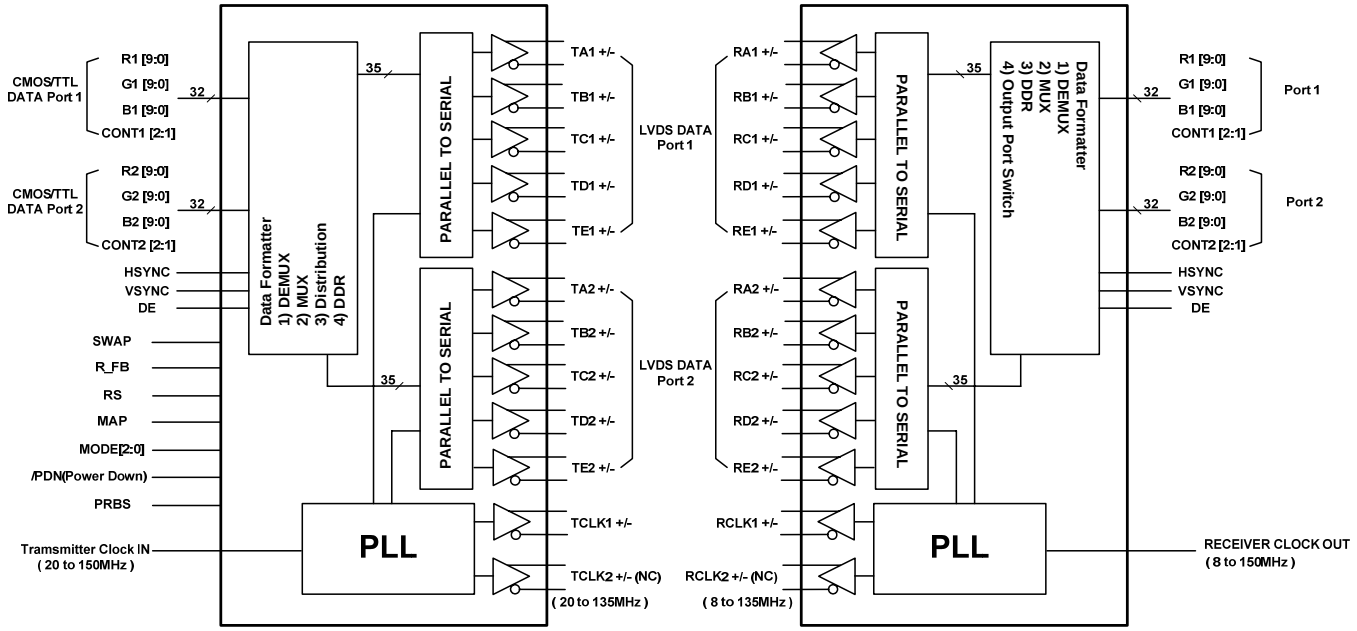

Figure 2. FPD Link Chipset for 60-Bit Color

Bit Mapping of FPD Interface Data

The transmitter's data input from the graphic controller consist of 18bits of video information, a horizontal synchronization bit, a vertical synchronization bit, and as enable bit for 18-bits device, or consist of 24bits of video information, a horizontal synchronization bit, a vertical synchronization bit, and as enable bit for 24-bits device, or consist of 30bits of video information, a horizontal synchronization bit, a vertical synchronization bit, and as enable bit for 30-bits device, or consist of 60bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bits, and a spare bit for 60bit device. Only three LVDS data channels are required for an 18-bit FPD interface application while a 24-bit application use 4 LVDS data channel, 30-bit application use 5 LVDS data channel and 60-bit application use 10 LVDS data channel. The most significant bits (MSB) for an 18-bit application, 24-bit application and 30-bit application must be mapped exactly the same as the most significant bits in the 60-bit application, and additional least significant in the 60-bit application are mapped the 10th LVDS data channel. The output of the receiver to LCD to panel controller has same bit mapping as the input the transmitter.

The detailed bit mapping information between the RGB data of graphic information and the CMOS/TTL data pins of the transmitter/receiver is listed in Table 1, 2 and that between the data arrangement of LVDS channels and the CMOS/TTL data pins of the transmitter/receiver is also described in Figure 3, Figure 4 and Figure 5.

Table 1. TX Bit Mapping for 18-bit, 24bit, 30-bit, 60bit Color Display

	VGA-TFT Even Data Signal			Transmitter Input Even Data Pin			VGA-TFT Odd Data Signal			Transmitter Input Odd Data Pin		
	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
LSB	RE0			R10			RO0			R20		
	RE1			R11			RO1			R21		
	RE2	RE0		R12	R12		RO2	RO0		R22	R22	
	RE3	RE1		R13	R13		RO3	RO1		R23	R23	
	RE4	RE2	RE0	R14	R14	R14	RO4	RO2	RO0	R24	R24	R24
	RE5	RE3	RE1	R15	R15	R15	RO5	RO3	RO1	R25	R25	R25
	RE6	RE4	RE2	R16	R16	R16	RO6	RO4	RO2	R26	R26	R26
	RE7	RE5	RE3	R17	R17	R17	RO7	RO5	RO3	R27	R27	R27
	RE8	RE6	RE4	R18	R18	R18	RO8	RO6	RO4	R28	R28	R28
MSB	RE9	RE7	RE5	R19	R19	R19	RO9	RO7	RO5	R29	R29	R29
LSB	GE0			G10			GO0			G20		
	GE1			G11			GO1			G21		
	GE2	GE0		G12	G12		GO2	GO0		G22	G22	
	GE3	GE1		G13	G13		GO3	GO1		G23	G23	
	GE4	GE2	GE0	G14	G14	G14	GO4	GO2	GO0	G24	G24	G24
	GE5	GE3	GE1	G15	G15	G15	GO5	GO3	GO1	G25	G25	G25
	GE6	GE4	GE2	G16	G16	G16	GO6	GO4	GO2	G26	G26	G26
	GE7	GE5	GE3	G17	G17	G17	GO7	GO5	GO3	G27	G27	G27
	GE8	GE6	GE4	G18	G18	G18	GO8	GO6	GO4	G28	G28	G28
MSB	GE9	GE7	GE5	G19	G19	G19	GO9	GO7	GO5	G29	G29	G29
LSB	BE0			B10			BO0			B20		
	BE1			B11			BO1			B21		
	BE2	BE0		B12	B12		BO2	BO0		B22	B22	
	BE3	BE1		B13	B13		BO3	BO1		B23	B23	
	BE4	BE2	BE0	B14	B14	B14	BO4	BO2	BO0	B24	B24	B24
	BE5	BE3	BE1	B15	B15	B15	BO5	BO3	BO1	B25	B25	B25
	BE6	BE4	BE2	B16	B16	B16	BO6	BO4	BO2	B26	B26	B26
	BE7	BE5	BE3	B17	B17	B17	BO7	BO5	BO3	B27	B27	B27
	BE8	BE6	BE4	B18	B18	B18	BO8	BO6	BO4	B28	B28	B28
MSB	BE9	BE7	BE5	B19	B19	B19	BO9	BO7	BO5	B29	B29	B29

Table 2. RX Bit Mapping for 18-bit, 24bit, 30-bit, 60bit Color Display

	TFT Panel Even Data			Receiver Output Even Data Pin			TFT Panel Odd Data			Receiver Output Odd Data Pin		
	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
LSB	RE0			R10			RO0			R20		
	RE1			R11			RO1			R21		
	RE2	RE0		R12	R12		RO2	RO0		R22	R22	
	RE3	RE1		R13	R13		RO3	RO1		R23	R23	
	RE4	RE2	RE0	R14	R14	R14	RO4	RO2	RO0	R24	R24	R24
	RE5	RE3	RE1	R15	R15	R15	RO5	RO3	RO1	R25	R25	R25
	RE6	RE4	RE2	R16	R16	R16	RO6	RO4	RO2	R26	R26	R26
	RE7	RE5	RE3	R17	R17	R17	RO7	RO5	RO3	R27	R27	R27
	RE8	RE6	RE4	R18	R18	R18	RO8	RO6	RO4	R28	R28	R28
MSB	RE9	RE7	RE5	R19	R19	R19	RO9	RO7	RO5	R29	R29	R29
LSB	GE0			G10			GO0			G20		
	GE1			G11			GO1			G21		
	GE2	GE0		G12	G12		GO2	GO0		G22	G22	
	GE3	GE1		G13	G13		GO3	GO1		G23	G23	
	GE4	GE2	GE0	G14	G14	G14	GO4	GO2	GO0	G24	G24	G24
	GE5	GE3	GE1	G15	G15	G15	GO5	GO3	GO1	G25	G25	G25
	GE6	GE4	GE2	G16	G16	G16	GO6	GO4	GO2	G26	G26	G26
	GE7	GE5	GE3	G17	G17	G17	GO7	GO5	GO3	G27	G27	G27
	GE8	GE6	GE4	G18	G18	G18	GO8	GO6	GO4	G28	G28	G28
MSB	GE9	GE7	GE5	G19	G19	G19	GO9	GO7	GO5	G29	G29	G29
LSB	BE0			B10			BO0			B20		
	BE1			B11			BO1			B21		
	BE2	BE0		B12	B12		BO2	BO0		B22	B22	
	BE3	BE1		B13	B13		BO3	BO1		B23	B23	
	BE4	BE2	BE0	B14	B14	B14	BO4	BO2	BO0	B24	B24	B24
	BE5	BE3	BE1	B15	B15	B15	BO5	BO3	BO1	B25	B25	B25
	BE6	BE4	BE2	B16	B16	B16	BO6	BO4	BO2	B26	B26	B26
	BE7	BE5	BE3	B17	B17	B17	BO7	BO5	BO3	B27	B27	B27
	BE8	BE6	BE4	B18	B18	B18	BO8	BO6	BO4	B28	B28	B28
MSB	BE9	BE7	BE5	B19	B19	B19	BO9	BO7	BO5	B29	B29	B29

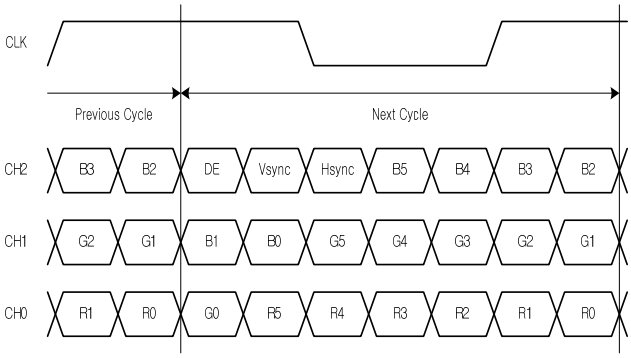

Figure 3. Bit Mapping between LVDS and CMOS/TTL signals for 18-bit Color Display

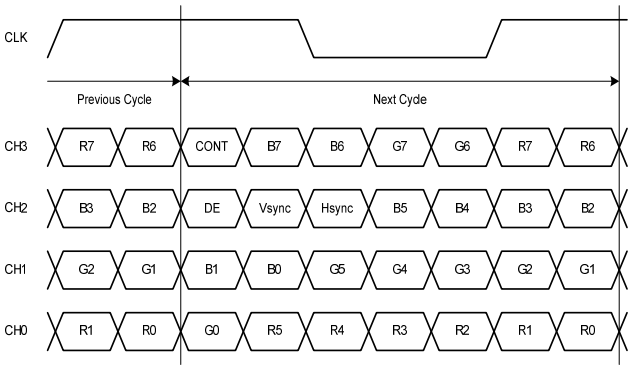

Figure 4. Bit Mapping between LVDS and CMOS/TTL signals for 24-bit Color Display

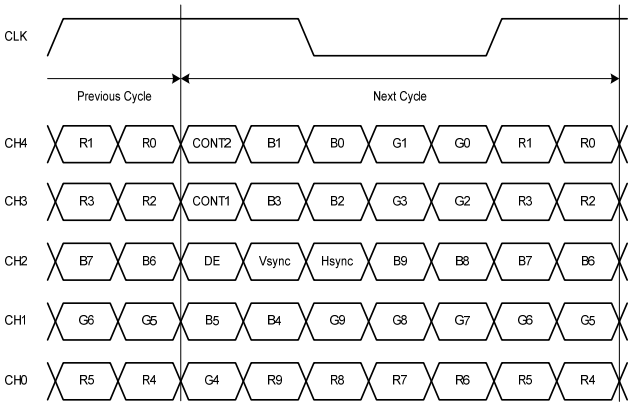

Figure 5. Bit Mapping between LVDS and CMOS/TTL signals for 30-bit Color Display

System Designing Considerations

PCB Layout Considerations

- Lines of a LVDS differential signal pair should always be adjacent to eliminate noise interference from other signals and make effectively the noise canceling of the differential signals.
- The physical length of PCB trace for a given LVDS differential signal pair should be matched as equal as possible.
- The physical length of PCB trace for each LVDS differential signal pairs should be keep as close to the same as possible.
- The physical length of PCB trace for each LVDS differential signal pairs should be keep as short as possible; otherwise the differential impedance of PCB must be controlled to be near 100 Ohm.

  The physical length of PCB trace of CMOS/TTL signals should be keep as short and close to the same as possible.
- The PCB trace of CMOS/TTL signals should be isolated from LVDS differential signal pairs, placing them at least “3s” or “2w” away (see Figure 6).
- To limit the impedance discontinuities causing signal reflection and crosstalk, the 90° angle on PCB trace must be not used (see Figure 7) and the number of via should be reduced.
- If any impedance discontinuities occur on one signal line, it must be mirrored in the other line of the differential pair.
- These considerations reduce the signal reflection and crosstalk, and make helpful to obtain full benefit of the noise and EMI reduction from LVDS.

Cables & Connectors

- In general, twinax or twisted pair cables are recommended.
- The shielded cable will diminish noise emissions and ground lines between each differential pair will provide a barrier to noise

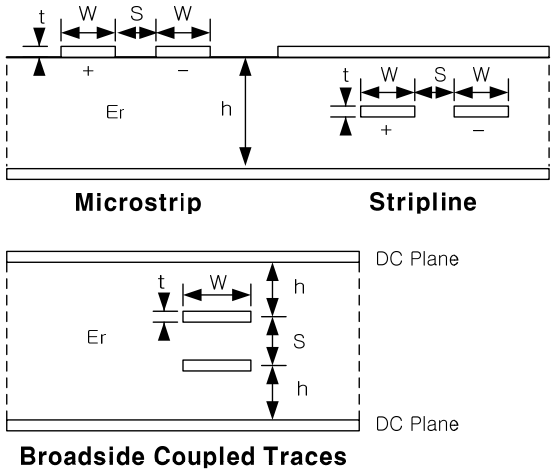

Figure 6. PCB Construct Cross-section

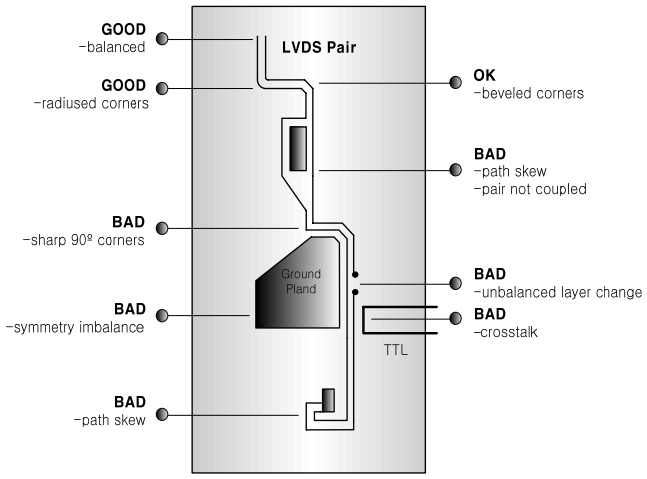

Figure 7. PCB Layout Example

coupling between adjacent pairs, thus contribute to reduce the noise and EMI.

- In addition, the low impedance ground connection between the transmitter and the receiver provides a return path for the common mode noise.
- In multi-row connectors, each differential pair signals should be placing on the same row to help minimize skew.
- Especially for high frequency and higher pin-count applications, LVDS-type cable assemblies such as 3M™ MDR and Amphenol SKEWCLEAR® systems are commonly recommended.

Termination

- Because of using current mode output driver in LVDS, a termination resistor is required across the receiver's differential input pair per a channel and its typical value is 100 Ohms (see Figure 8).
- These termination resistors should be placing as close as possible to the receiver's input pins

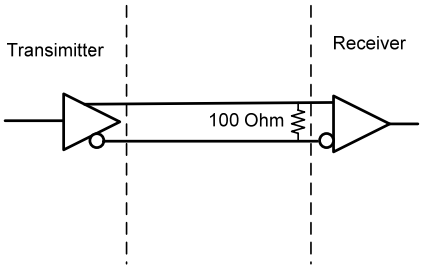

Figure 8. LVDS Differential Termination

to shorten stubs and effectively terminate the differential lines.

- For the type of resistor, surface mount resistors are recommended rather than leaded resistors to avoid additional parasitic inductance.

Power & Ground

- Power supply system performance can be greatly improved by bypassing capacitors that reduce the impact of switching noise and its feedback or interference between different blocks of the circuits (see Figure 9).
- In general, each VCC pins are required to have separate bypassing sufficient to ensure less than 100 mV peak-to-peak noises on supply pins,

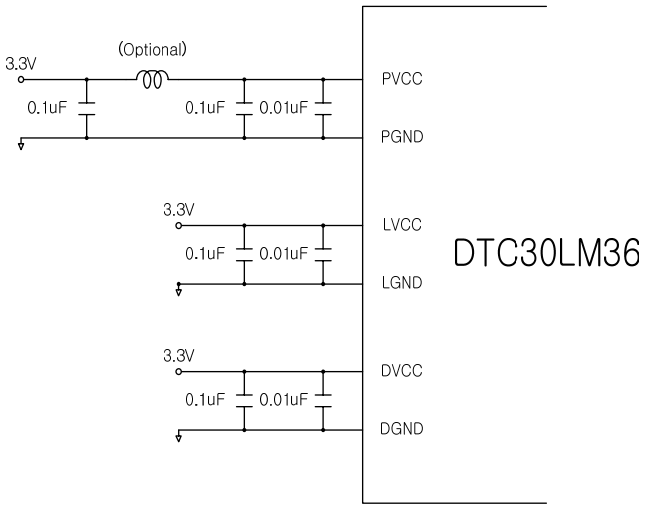

Figure 9. Typical Power Supply Bypassing Configuration

especially PVCC.

Power Up Sequencing

- A specific power up sequence is not required in the DTC FPD Interface chipset family. But the best practice is: power up all VCC together, apply clocks, and then assert /PDN power-down pins high to enable the transmitter and/or receiver.
- The /PDN pin is internally pulled down to ground that the device is disabled if this pin is left open circuited.
- When powering down the device, the transmitter outputs remain in tri-state and the receiver outputs are low.
- When the device are actively driven, the /PDN pin should be pulled up to VCC by no more than a 10 kOhms resistor.

Data Strobe Selection

- The DTC FPD transmitters are available with data strobe selection, a rising or falling edge. It can be selected based on the characteristics of the VGA controller being used.
- The DTC FPD receivers are available with either a falling edge data strobe or a rising edge data strobe, which device may be selectable according to the LCD panel timing controller requirements. The strobe edge only affects the TTL inputs of the transmitter or outputs of the receiver, while the LVDS interface is not effected.

Clock Jitter Considerations

- The DTC FPD Interface chipset family employs a PLL to generate and recover the clock used in the transmission across the LVDS interface because its high speed signals require an accurate, low noise clock signal.
- The time width of the LVDS data bits is one seventh the clock period. For example, a clock of frequency 65 MHz has a period of 15.4 ns; the time width of a data bit is 2.2 ns.
- However, all of differential signal skew, interconnect skew, data and clock jitter reduce the available window for sampling data. Thus, it is recommended to keep each component as small as possible to support the maximum operating frequency.

Other Benefits

- Other benefits of the LVDS technology employed in the DTC FPD Interface are the relatively low EMI and simpler physical interface.
- LVDS has demonstrated lower EMI than other competing technologies such as RS-422, PECL and CMOS, often used in display interface applications.
- The conversion from parallel TTL to serial LVDS allows for a simpler interface between

graphic controller and LCD panel, which means a lower cable cost and a simple physical connection through a notebook hinge are available.

Conclusion

- The DTC FPD Interface chipset architecture in conjunction with the LVDS technology provides the high-end interface necessary for the leading edge of flat panel display technology, and further on, will provide optimal solutions for the industry's ever increasing needs for high-end display technology.

IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.