LVDS Product

DTC LVDS Products Application Note (*Preliminary Ver. 1.3*)

LVDS Flat Panel Display (FPD) Interface Transmitter/Receiver - 85MHz

Introduction

The DTC FPD Interface chipsets are the family of flat panel display system's interface devices specially configured to provide high-quality data transmission between graphic controller and LCD panels with high speed, low power and low EMI considerations as well as simpler physical interface concern. For these purpose, the DTC FPD Interface chipset family employs the LVDS (Low Voltage Differential Signaling) technology and offers better efficient method for high-end FPD system such as SVGA (800x600) and XGA (1024x768).

This application note's purpose is not to specify a strict circuit implementation of a display system using the DTC FPD Interface chipset family, but to provide some guidelines for successful implementation of it.

System Description

The example of typical display system using the DTC FPD interface chipset family is consist of transmitters and receivers (see Figure 1), interconnected over a cable including three or four twisted-pair data signal wires, one twisted-pair clock signal wires, a power wire and a ground wire. The DTC FPD interface chipset family includes devices to support 18-bit and 24-bit color displays, a frequency range of 20 MHz to 85 MHz, and alternative selection of rising or falling edge for data and control strobe (see Figure 2).

Note: For more detailed information about the DTC FPD interface chipset, see the data sheets for DTC34LM85 and DTC34LF86/DTC34LR86

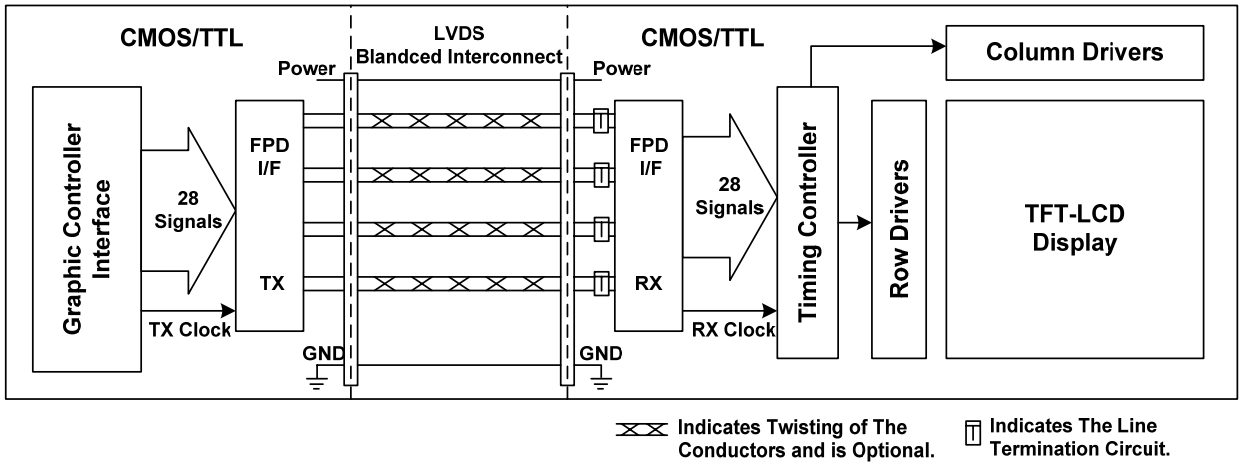

Figure 1. Typical FPD Link Application (24-Bit Color)

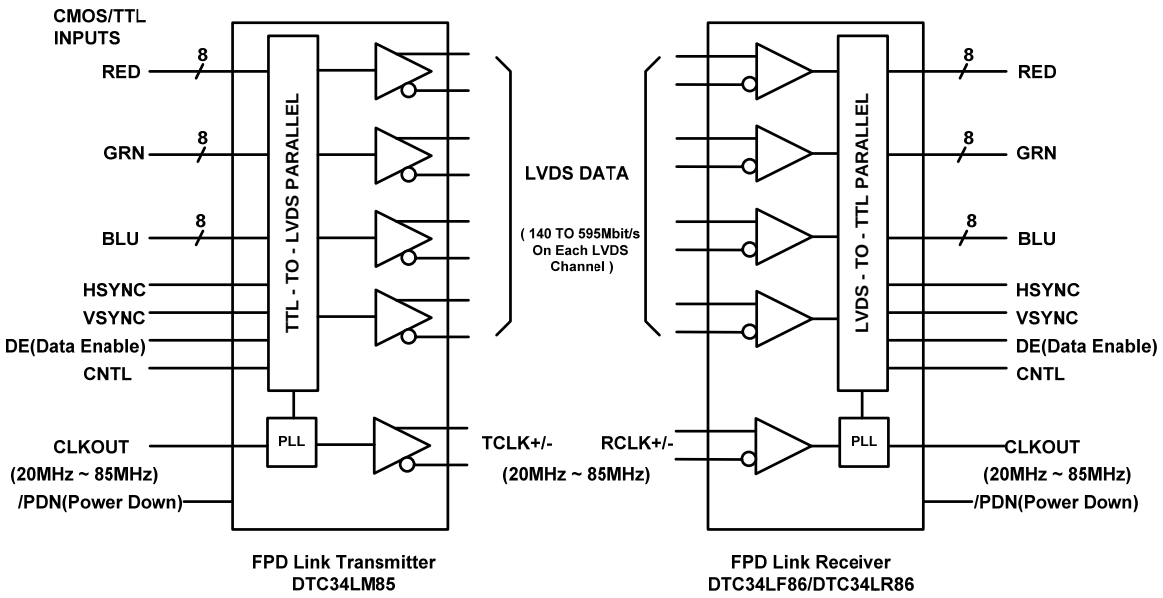

Figure 2. FPD Link Chipset for 24-Bit Color

Bit Mapping of FPD Interface Data

The transmitter's data input from the graphic controller consist of 18 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, and an enable bit for 18-bit device, or consist of 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit , and a spare bit for 24-bit device. Only three LVDS data channels are required for an 18-bit FPD interface application while a 24-bit application use 4 LVDS data channel. The most significant bits (MSB) for an 18-bit application must be mapped exactly the same as the most significant bits in the 24-bit application, and additional least significant in the 24-bit application are mapped the 4th LVDS data channel. The output of the receiver to LCD panel controller has same bit mapping as the input to the transmitter.

The detailed bit mapping information between the RGB data of graphic information and the CMOS/TTL data pins of the transmitter/receiver is listed in Table 1, and that between the data arrangement of LVDS channels and the CMOS/TTL data pins of the transmitter/receiver is also described in Figure 3 and Figure 4.

Table 1. Bit Mapping for 18-bit and 24-bit Color Display

VGA-TFT Data Signal			Transmitter Input Data Pin		Receiver Output Data Pin		TFT Panel Data Signal	
	24-bit	18-bit	24-bit Tx (34LM85)	18-bit Tx (33LM85)	24-bit Rx (34LF/LR86)	18-bit Rx (33LF/LR86)	18-bit	24-bit
LSB	R0		TX0		RX0			R0
	R1		TX1		RX1			R1
	R2	R0	TX2	TX0	RX2	RX0	R0	R2
	R3	R1	TX3	TX1	RX3	RX1	R1	R3
	R4	R2	TX4	TX2	RX4	RX2	R2	R4
	R5	R3	TX6	TX3	RX6	RX3	R3	R5
	R6	R4	TX27	TX4	RX27	RX4	R4	R6
MSB	R7	R5	TX5	TX5	RX5	RX5	R5	R7
LSB	G0		TX7		RX7			G0
	G1		TX8		RX8			G1
	G2	G0	TX9	TX6	RX9	RX6	G0	G2
	G3	G1	TX12	TX7	RX12	RX7	G1	G3
	G4	G2	TX13	TX8	RX13	RX8	G2	G4
	G5	G3	TX14	TX9	RX14	RX9	G3	G5
	G6	G4	TX10	TX10	RX10	RX10	G4	G6
MSB	G7	G5	TX11	TX11	RX11	RX11	G5	G7
LSB	B0		TX15		RX15			B0
	B1		TX18		RX18			B1
	B2	B0	TX19	TX12	RX19	RX12	B0	B2
	B3	B1	TX20	TX13	RX20	RX13	B1	B3
	B4	B2	TX21	TX14	RX21	RX14	B2	B4
	B5	B3	TX22	TX15	RX22	RX15	B3	B5
	B6	B4	TX16	TX16	RX16	RX16	B4	B6
MSB	B7	B5	TX17	TX17	RX17	RX17	B5	B7
	RSVD		TX23		RX23			RSVD
	Hsync	Hsync	TX24	TX18	RX24	RX18	Hsync	Hsync
	Vsync	Vsync	TX25	TX19	RX25	RX19	Vsync	Vsync
	DE	DE	TX26	TX20	RX26	RX20	DE	DE

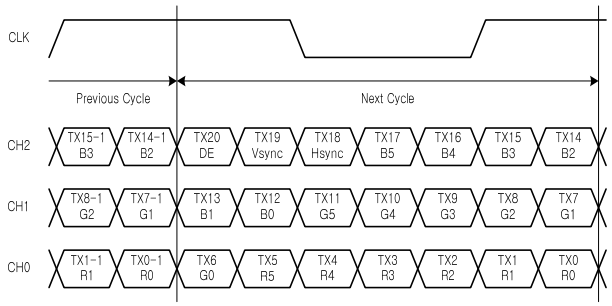

Figure 3. Bit Mapping between LVDS and CMOS/TTL signals for 18-bit Color Display

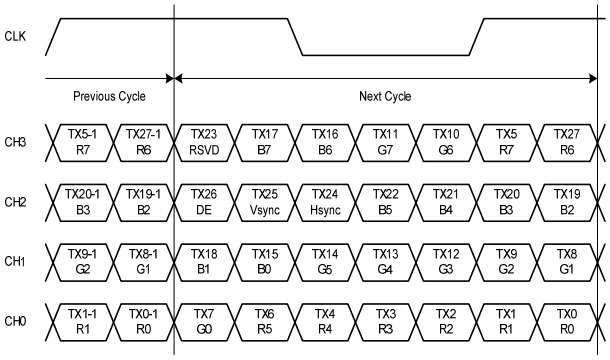

Figure 4. Bit Mapping between LVDS and CMOS/TTL signals for 24-bit Color Display

System Designing Considerations

PCB Layout Considerations

- Lines of a LVDS differential signal pair should always be adjacent to eliminate noise interference from other signals and make effectively the noise canceling of the differential signals.
- The physical length of PCB trace for a given LVDS differential signal pair should be matched as equal as possible.
- The physical length of PCB trace for each LVDS differential signal pairs should be keep as close to the same as possible.
- The physical length of PCB trace for each LVDS differential signal pairs should be keep as short as possible; otherwise the differential impedance of PCB must be controlled to be near 100 Ohm.

  The physical length of PCB trace of CMOS/TTL signals should be keep as short and close to the same as possible.
- The PCB trace of CMOS/TTL signals should be isolated from LVDS differential signal pairs, placing them at least “3s” or “2w” away (see Figure 5).
- To limit the impedance discontinuities causing signal reflection and crosstalk, the 90° angle on PCB trace must be not used (see Figure 6) and the number of via should be reduced.
- If any impedance discontinuities occur on one signal line, it must be mirrored in the other line of the differential pair.
- These considerations reduce the signal reflection and crosstalk, and make helpful to obtain full benefit of the noise and EMI reduction from LVDS.

Cables & Connectors

- In general, twinax or twisted pair cables are recommended.
- The shielded cable will diminish noise emissions and ground lines between each differential pair will provide a barrier to noise

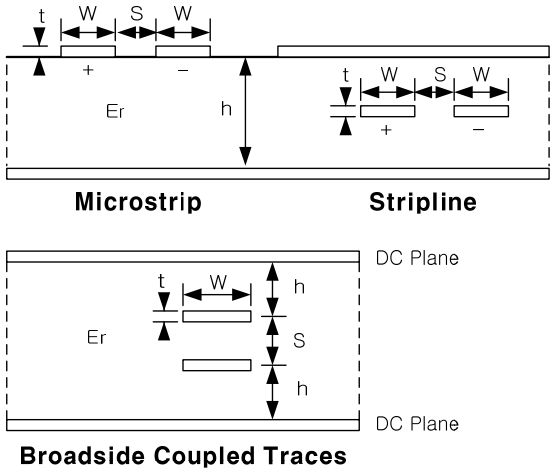

Figure 5. PCB Construct Cross-section

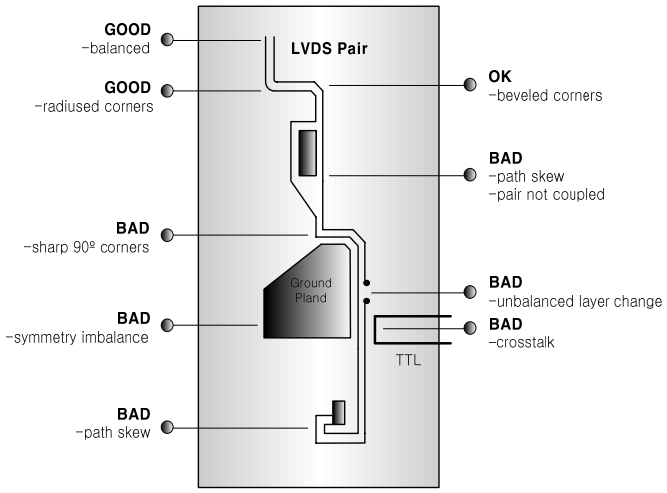

Figure 6. PCB Layout Example

coupling between adjacent pairs, thus contribute to reduce the noise and EMI.

- In addition, the low impedance ground connection between the transmitter and the receiver provides a return path for the common mode noise.
- In multi-row connectors, each differential pair signals should be placing on the same row to help minimize skew.
- Especially for high frequency and higher pin-count applications, LVDS-type cable assemblies such as 3M™ MDR and Amphenol SKEWCLEAR® systems are commonly recommended.

Termination

- Because of using current mode output driver in LVDS, a termination resistor is required across the receiver's differential input pair per a channel and its typical value is 100 Ohms (see Figure 7).
- These termination resistors should be placing as close as possible to the receiver's input pins

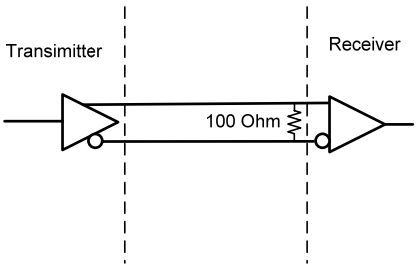

Figure 7. LVDS Differential Termination

to shorten stubs and effectively terminate the differential lines.

- For the type of resistor, surface mount resistors are recommended rather than leaded resistors to avoid additional parasitic inductance.

Power & Ground

- Power supply system performance can be greatly improved by bypassing capacitors that reduce the impact of switching noise and its feedback or interference between different blocks of the circuits (see Figure 8).
- In general, each VCC pins are required to have separate bypassing sufficient to ensure less than 100 mV peak-to-peak noises on supply pins,

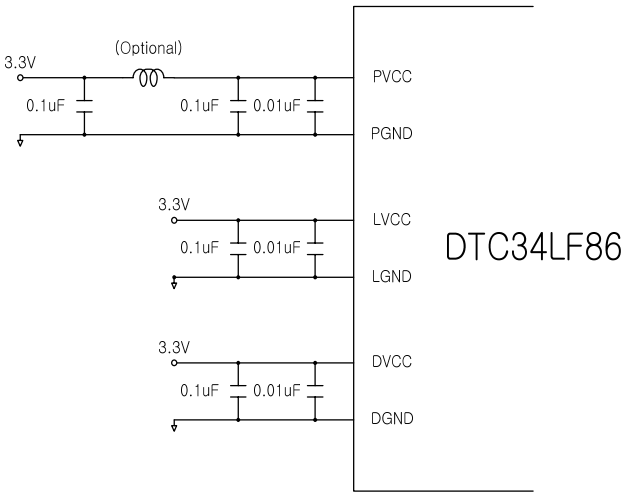

Figure 8. Typical Power Supply Bypassing Configuration

especially PVCC.

Power Up Sequencing

- A specific power up sequence is not required in the DTC FPD Interface chipset family. But the best practice is: power up all VCC together, apply clocks, and then assert /PDN power-down pins high to enable the transmitter and/or receiver.
- The /PDN pin is internally pulled down to ground that the device is disabled if this pin is left open circuited.
- When powering down the device, the transmitter outputs remain in tri-state and the receiver outputs are low.
- When the device are actively driven, the /PDN pin should be pulled up to VCC by no more than a 10 kOhms resistor.

Data Strobe Selection

- The DTC FPD transmitters are available with data strobe selection, a rising or falling edge. It can be selected based on the characteristics of the VGA controller being used.
- The DTC FPD receivers are available with either a falling edge data strobe or a rising edge data strobe, which device may be selectable according to the LCD panel timing controller requirements. The strobe edge only affects the TTL inputs of the transmitter or outputs of the receiver, while the LVDS interface is not effected.

Clock Jitter Considerations

- The DTC FPD Interface chipset family employs a PLL to generate and recover the clock used in the transmission across the LVDS interface because its high speed signals require an accurate, low noise clock signal.
- The time width of the LVDS data bits is one seventh the clock period. For example, a clock of frequency 65 MHz has a period of 15.4 ns; the time width of a data bit is 2.2 ns.
- However, all of differential signal skew, interconnect skew, data and clock jitter reduce the available window for sampling data. Thus, it is recommended to keep each component as small as possible to support the maximum operating frequency.

Other Benefits

- Other benefits of the LVDS technology employed in the DTC FPD Interface are the relatively low EMI and simpler physical interface.
- LVDS has demonstrated lower EMI than other competing technologies such as RS-422, PECL and CMOS, often used in display interface applications.
- The conversion from parallel TTL to serial LVDS allows for a simpler interface between

graphic controller and LCD panel, which means a lower cable cost and a simple physical connection through a notebook hinge are available.

Conclusion

- The DTC FPD Interface chipset architecture in conjunction with the LVDS technology provides the high-end interface necessary for the leading edge of flat panel display technology, and further on, will provide optimal solutions for the industry's ever increasing needs for high-end display technology.

IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.